MICROPROCESSOR - BASED POWER SYSTEM TELEMETRY THROUGH FIBRE - OPTIC LINK

A Thesis Submitted

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By

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CERTIFICATE

Certified that this work 'Microprocessor Based Power System Telemetry Through Fibre-Optic Link' by Abhijit Ganguly is carried under my supervision and is not submitted for a degree elsewhere.

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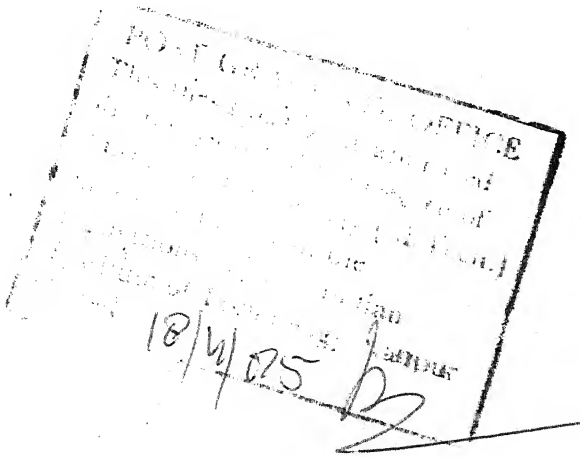

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I am also thankful to Mr.Joseph John and Mr.Goutem Deb for maintaining perfect working conditions in the laboratory.

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-Abhijit Ganguly

TABLE OF CONTENTS

LIST OF FIGURES

ABSTRACT

The work reported in this thesis deals with the Telemetry of Power Systems Parameters from generating stations or sub-stations to a master control station for monitoring and control purposes.

A transmitter was designed and implemented to acquire data related to the different parameters, process it in a 8-bit microprocessor and transmit it to the master control station through a short optical fibre link.

A receiver was designed and implemented for the master control station which could take care of the message received from a number of such transmitters that may be connected to it through the link.

The fibre optic communication link used has a LED source and PIN photodetector.

CHAPTER 1

INTRODUCTION

1.1 What is Telemetry

Telemetry, by definition, is the collecting of data from inaccessible locations and transmitting the information to accessible locations. Today the concept of Telemetry system has been broadened to include actuation of devices and systems from a remote location. Thus Telemetry systems find wide applications where centralised control of widely dispersed units is required. Telemetry systems are used in many and varied applications like satellite control and communication, aircraft communication, submarine communication, oil-fields, mines, electric-power generation and distribution etc. This thesis, as the title suggests, deals with telemetry applications in the last of the above mentioned areas.

1.2 Advantage of Using Telemetry for Power Systems

The Telemetry systems are essentially data acquisition systems for acquiring data from complex systems which are generally distributed geographically over a vast area. Power system with its inherent distributed nature lends itself as ideal application area for Telemetry system. With ever increasing demand for electrical energy coupled with the recent energy crises faced all over the world, the efficiency in generation and distribution of electrical

energy has become an increasingly important criterion. Further the interconnection of electrical distribution grids at area, region and national level to provide an integrated distributed network has added an additional dimension, to the over-all complexity of the electrical network. This in turn requires finer monitoring and control of various parameters of the distributed power system. The economic advantages of integrated management of large power systems network have been well established. The major benefits of such operation are the following:

(a) Reduction of installed capacity required to meet the varying load demands.

(b) Reduction in reserve capacity required.

(c) Ability to introduce large size generating units.

(d) Enhanced reliability of power supply.

A basic requirement in the management of such a large network, as the Power System, in an integrated manner is the ability to centrally monitor and control a large number of system parameters such as line voltages, currents, frequency, MW generation, load demand, circuit breaker positions, transformer tap positions etc., of the widely distributed generating stations, sub-stations and the transmission network. The volume and type of information to be exchanged will depend on factors such as levels of the

centres in the network hierarchy, monitoring and control functions assigned to the centres exchanging data and the extent of automation employed by the system. This exchange of information calls for a efficient communication system linking the whole network. Telemetry systems employing appropriate communication medium offer a versatile means of such remote monitoring and control of system parameters.

1.3 Drawback of Early Days Telemetry Systems

The telemetry technology has evolved over a considerable period of time. In the initial days, the conventional telemetry systems which were in use, have now become obsolete due to their inherent disadvantages. The conventional telemetry systems are based on hard-wired logic and use digital cyclic technique for monitoring and transmitting data for generating station (sub-stations to the controlling station or the Electric Load Despatch Centre (ELDC) as it is better known. These systems have the following limitations:

(a) Lack of operational flexibility.

(b) Size of hardwired circuitry is large.

(c) Data security is minimal.

(d) Diagnostic checking capability is minimal.

1.4 Modern Trends in Power System Telemetry

The advent of microprocessors have revolutionized telemetry and telecontrol systems. Computer-based telemetry systems are being currently used for monitoring and control of power systems. These consists of the following:

(a) A central computer system at the Master Control Station or ELDC.

(b) Remote terminal units (RTUs) placed at various generating stations/sub-stations.

(c) Dedicated communication channels between the Master Control Station and the RTUs.

The central computer system is generally built around a dual microcomputer system operating preferably in hot standby mode. Configuration of the system comprises system disks, logger printers, coloured semigraphic display units, key boards, mimics, communication interface, operator's console etc.

The RTU is a microprocessor - based data acquisition system suitable for Telemetry and Telecontrol applications. It is situated close to a number of measuring and control instruments of a generating station/sub-station from which the information is collected and to which control commands are passed. RTUs scans its inputs at predetermined time intervals, compares the readings with previously stored

data, thus enabling detection of change of state and alarms. This information is kept ready by the RTU for forward transmission to the central computer when called for. It employs sophisticated microprogramming technique to provide a highly secure method of data transmission and being soft-ware based offers a considerable degree of flexibility for incorporating special application - oriented features. The data transmission between the Master Station and the RTUs is effected by suitable communication protocols which ensure the data integrity.

The overall system consisting of the Master Control Station, RTUs and the communication links is called Supervisory Control and Data Acquisition (SCADA) system. There are other names used for such systems for example, communication, command and control system (c^3 systems). The name SCADA is preferred for such systems as the words 'Supervisory' and 'Control' describe the functions explicitly. The details of a SCADA system is given in the next chapter.

1.5 Need for Optical-Fibre Link in Power System Telemetry

In any communication network for an electric power system it is essential to prevent interference by electromagnetic fields produced by the very large voltages and currents, specially due to switching transients which are carried by the electric power cables. In this regard, the

twisted pair cables are not suitable as they are very much prone to disturbances by such noises. The preferred solution in the past has been micro-wave free space propagation, but the construction of plycns for the micro-wave antenna near the ultra-high voltage underground transformer sub-stations in the city is very difficult and expensive. In addition radio-wave blocking by high rise buildings has always been a major factor. With optical fibre there is no such problems and hence fibre optic link is best suited for power system telemetry.

Today optical-fibre communication systems for telemetry purposes have entered the phase of actual use at several power companies in Japan. More facts about this can be had from the paper titled, 'Optical-Fibre Communications for Electric Power Companies in Japan' appearing in the October 1980 issue of the IEEE Proceedings (1).

The need for optical fibre communication systems for the power companies are tabulated in Table 1.1. From the table, it is clear that the main competition of the fibre optic, as a link, is with electric wire. Below a comparison is given between electrical wire and fibre optics.

Table 1.1

Need for future data transmission systems	Problem Besetting current system	Solution	Difficulty of solution	Need for Optical Fiber Communication system
1. High reliability and high quality data transmission	1. Coax. or carrier systems:			Hitherto unsolved technical bottlenecks may be completely solved by fully exploiting the features of the fibre optic communication system
2. Large capacity data transmission	a. Transmission failure and interruption due to electromagnetic interference	a. Use of aluminium shielded cable	There is a limit to solution	
	b. Destruction of electronic circuits due to abnormal voltage surge	b. Duplicated system design using standby route	-do-	(a) Non-inductivity (b) High insulation property
	c. Increase in underground conduits for installation of cables	c. Installation of safety device	-do-	(c) Large data transmission
		d. Enforcement of error check system		(d) Decrease in underground conduits
	2. Microwave communication system: Communication failure due to radio wave blocking of high rise building	Increasing tower height	-do-	

1.5.1 Electrical Wire Vs. Fibre Optics

Advantages:

(1) In fibre optic cables the signals are transmitted in the form of energy packets (photons) which have no electrical charge. Consequently it is physically impossible for high electric fields (lightning, high-voltage etc.) or large magnetic fields (heavy electrical machinery, transformers, cyclotron etc.) to affect the transmission.

(2) There can be a slight leakage of flux from an optical fibre, but shielding is easily done by an opaque jacket, so signal bearing fibres cannot interfere with each other or the most sensitive electric circuits, and the optically transmitted wave form is therefore secure from external detection.

(3) In some applications, optical fibres carry signals enough to be energetically useful (e.g. for photocoagulation) and potentially harmful. But in most data communication applications economy dictates the use of flux levels of 100 μ W or less. Such levels are radiologically safe and in the event of a broken or damaged cable, the escaping flux is

harmless in explosive environments where a spark from a broken wire could be disastrous.

(4) Jacketed fibre optic cables can tolerate more mechanical abuse (crush, impact, flexure) than electrical cables of comparable size. Moreover fibre optic cables have an enormous weight and size advantage - for equivalent information capacity.

(5) Properly cabled optical fibres can tolerate any kind of weather and can without ill-effect, be immersed in most fluids, including poulluted air and water.

(6) Bandwidth considerations clearly give the advantage to fibre optics. In either parallel - or coaxial-wire cable, the bandwidth varies inversely as the square of the length. While in fibre-optic cable it varies inversely as only the first power of the length.

Disadvantages:

The only disadvantage, worth-mentioning, that fibre-optics have as compared to wire cables is that the later may have several signal 'taps', but multiple taps on fibre optic cables are economically impractical at present.

The above mentioned features are exploited to the utmost for power system telemetry. Table 1.2 shows by purpose how these features are best utilised.

1.6 Thesis Outline

In the next Chapter, i.e. Chapter 2, we describe in detail a SCADA system and the scope of the present work. In Chapter 3 the system design is considered. Chapters 4 and 5 deal with the hardware and the software of the system respectively. Finally conclusions and scope for further work is given in Chapter 6.

Table 1.2

Purpose of Use	Feature Utilized	
	Non-inductivity property	Large data transmission capacity
Power system protection	O	
Supervision & control	O	O
Inter-computers	O	O
General Communication	O	

O : Principally used features.

CHAPTER 2

OVERVIEW OF A SCADA SYSTEM

The functional block diagram of a SCADA system is given in Fig.2.1 which shows three RTUs connected to a Master Control Station. Three full-duplex data communication link is provided for the three RTUs together various data and transmit it to the Master Station, which in turn processes the data and sends back control command to the RTUs.

2.1 Network Configuration for SCADA Systems

Generally the following configurations are being used for SCADA systems:

(a) Point-to-point

(b) Star configuration

(c) Double-star configuration

(d) Star and multi-drop configuration

(a) Full Duplex Point-to-point Configurations

As shown in Fig.2.2, it provides two-way communication between one master and one remote station employing full duplex modes. Point-to-point configuration is simple but it requires independent telemetry trans-receiver for one

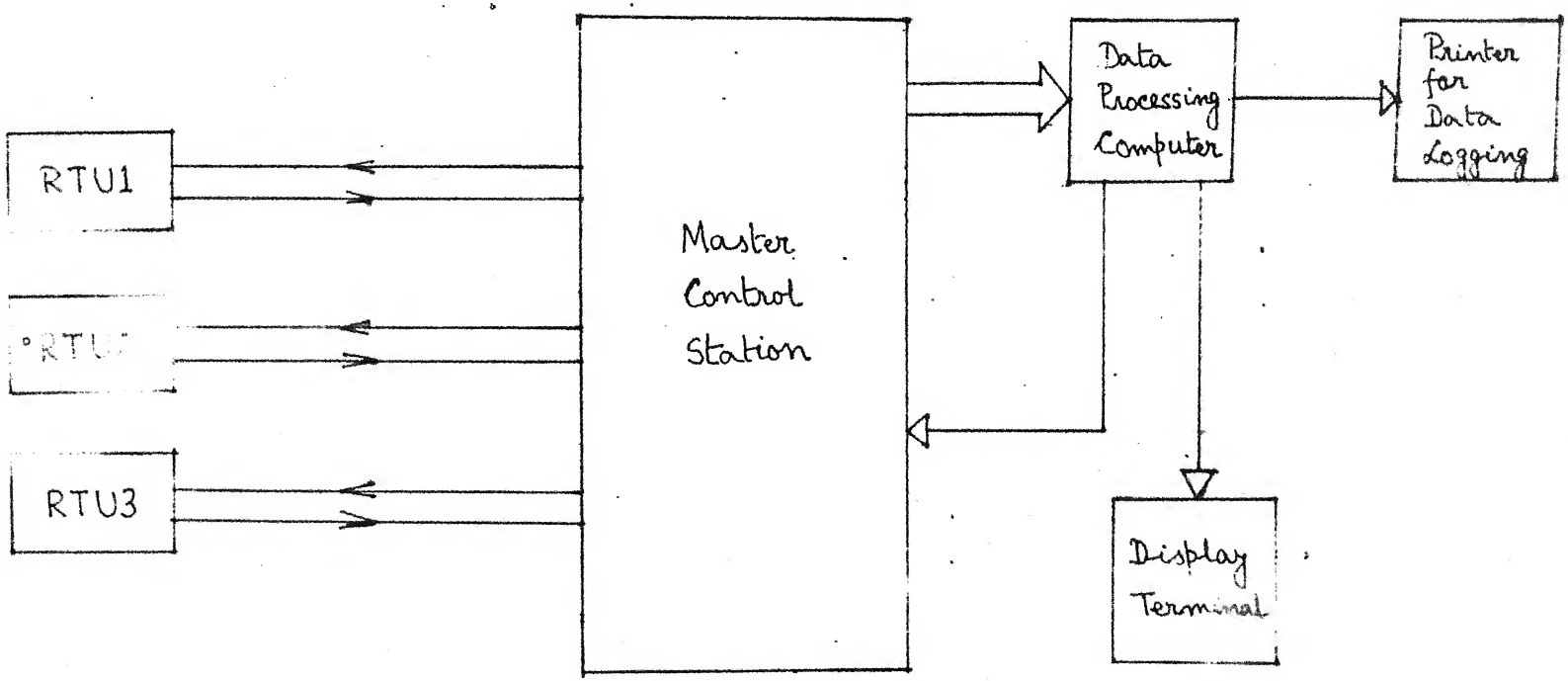

RTU1
RTU2
RTU3
Master Control Station
Data Processing Computer
Printer for Data Logging
Display Terminal

Fig. 2.1

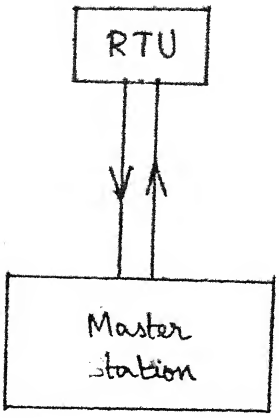


Fig. 2.2.

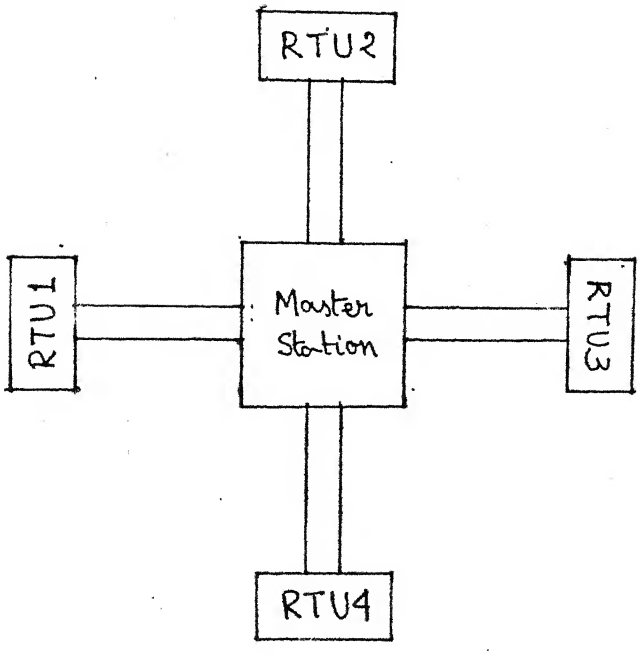


Fig. 2.3

data centre and many times it becomes uneconomical. Still in power systems where one or two remotely-located data centres are only there, point-to-point telemetry is used.

(b) Star-configured Full Duplex Telemetry Scheme

This arrangement, shown in Fig.2.3, is normally used for centralized control systems. In this case, even if one RTU fails, the other RTUs will be under the master station's control and the system is not much affected. However if the master station fails, the complete network fails and thus there is a need for hot standby units for the master station.

(c) Double Star Configuration

It is a two-level hierarchical star configuration. This configuration can be thought of as several RTUs connected in star mode to Auxillary Control Stations (ACS) which are connected to the master station again in star mode. Here again, for better system availability hot standby units have to be provided. This configuration is illustrated in Fig.2.4.

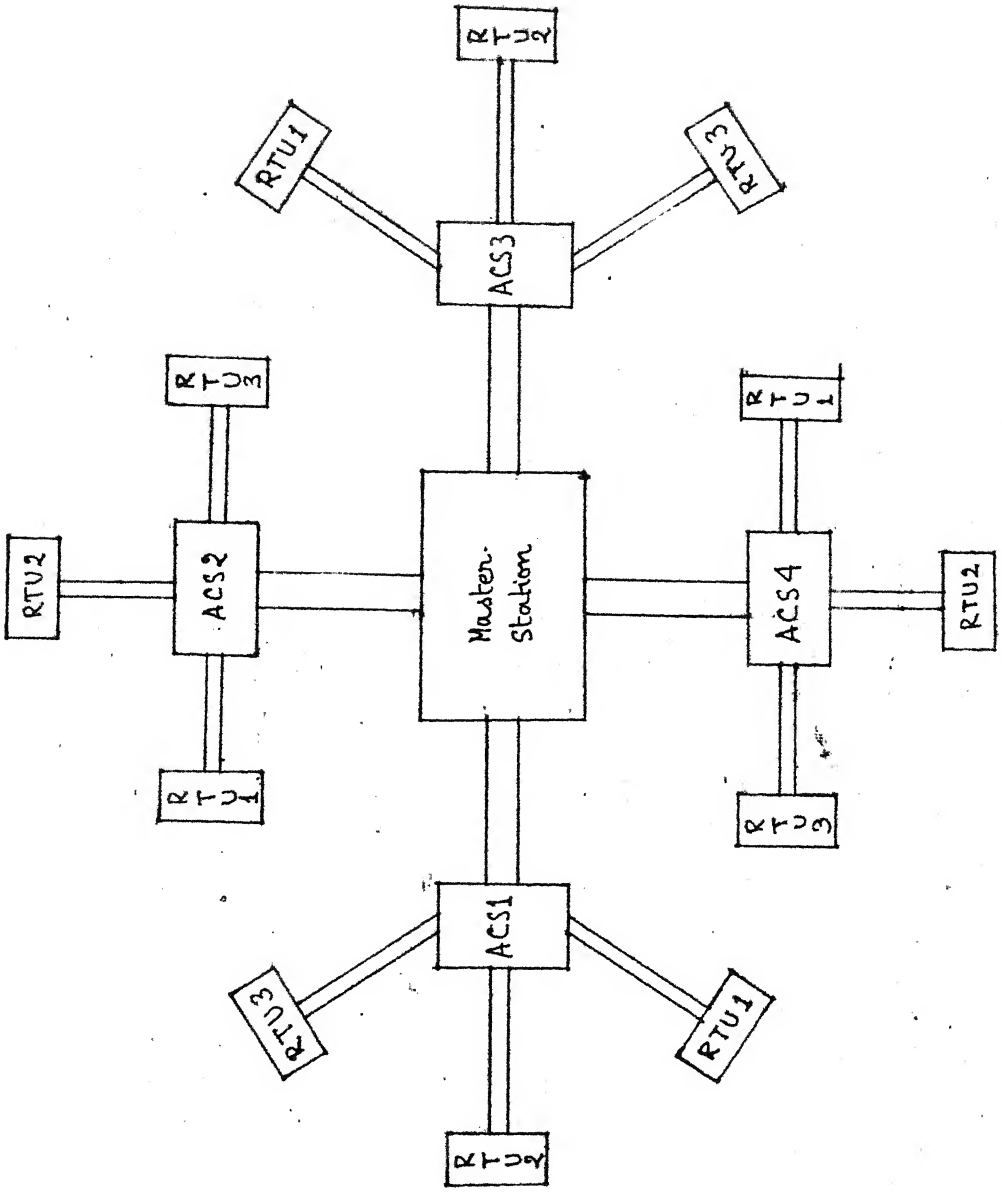

RTU2
RTU1
RTU3
ACS3
RTU3
RTU1
RTU2
ACS2
Master Station
ACS4
RTU2
RTU1
RTU3
ACS1
RTU3
RTU1
RTU2

Fig. 2.4

(d) Star and Multidrop Configuration

The configuration is shown in Fig.2.5. It uses an economic way of interconnecting RTUs and master stations. A prerequisite here is that a communication system must be available for this configuration.

2.2 Types of Data in Power Systems

Data generally measured in power systems for telemetry and telecontrol purposes are related to some of the following parameters:

(a) AC voltages and current
(b) Power
(c) Reactive power
(d) Line frequency
(e) Power factor
(f) Energy
(g) States of circuit brakers and transformer tap positions.

2.3 SCADA System-Hardware

(a) RTU:

Using appropriate transformers, the analog phase voltage and phase currents are converted into suitable low level voltages and fed as the analog input of the RTU. The digital inputs such as circuit braker (CB) status and

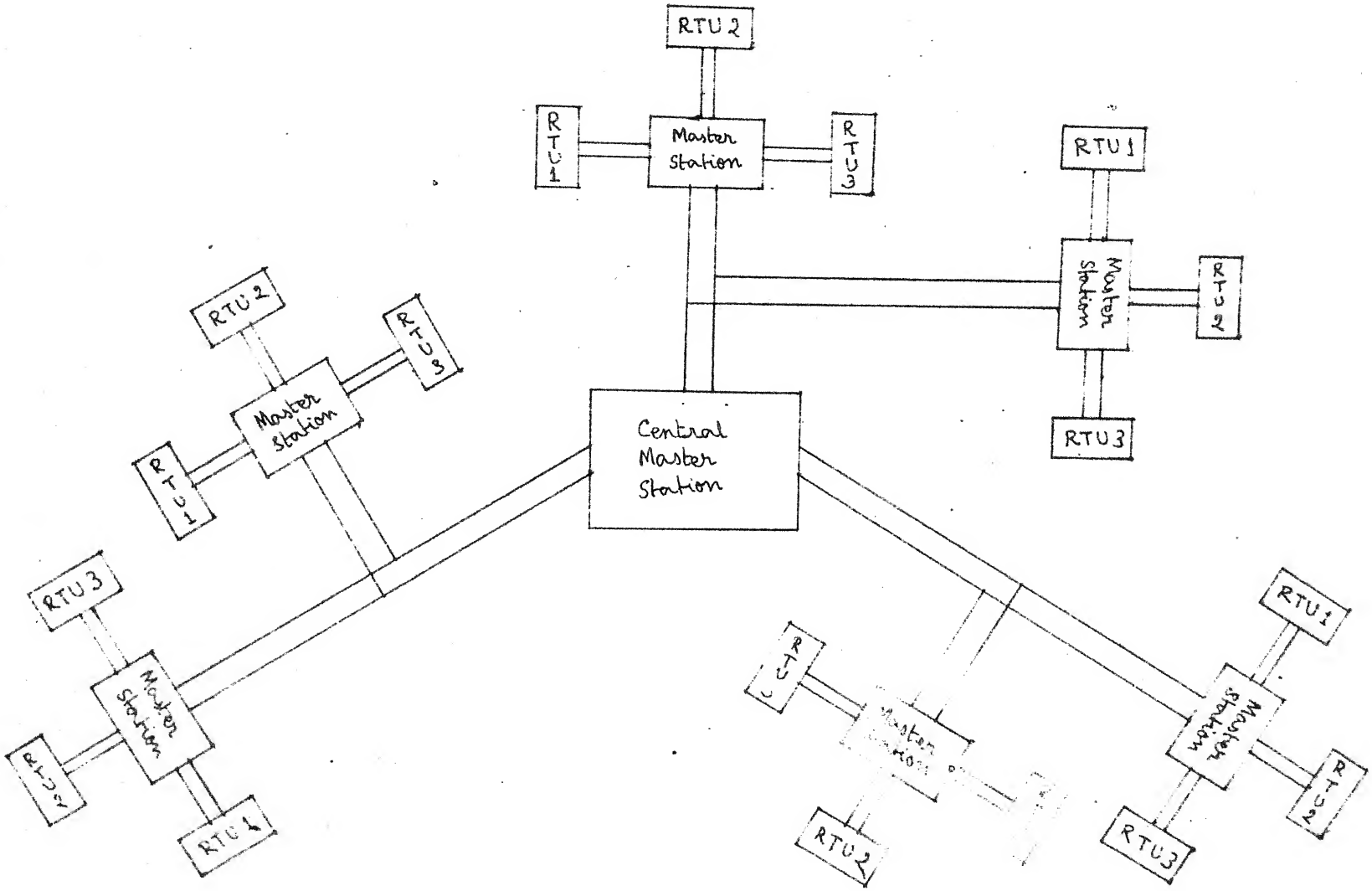

RTU 2
RTU 1
Master Station
RTU 3
RTU 1
Master Station
RTU 2
RTU 3
RTU 2
Master Station
RTU 3
Central Master Station
RTU 3
Master Station
RTU 1
RTU 1
RTU 2
RTU 1
RTU 3
RTU 2

Fig. 2.5

transformer tap positions are derived from potential free auxillary contacts of the corresponding CBs. Thus the RTUs contain isolation block, signal conditioning block, multiplexers, analog to digital converter, sample and hold, RAM, ROM, Microprocessor and Communication interface hardware elements. MOS circuitry is preferred as it is highly immune to noise. the RTUs are provided with self-diagnostic check bits and data format programmes stored in ROM for making the system smart. The command inputs are also decoded by RTUs and appropriate information is sent as per the Master Station's demand. The terminals are also provided with the input/output buffers to have a better transmission capability. The data are sent by block by block transmission rather than bit by bit transmission. A schematic representation of the RTU is given in Fig.2.6.

(b) Computer-based Master Station

Configuration of this comprises a minicomputer system comprising system disks, logger printers, coloured semi-graphic display units, Keyboards, mimics, communication interface, operator's console etc. The function of a typical central unit with all accessory equipments can be summarized as follows:

- Display and recording of the data transmitted by the RTUs.
- Recording and display of energy values.

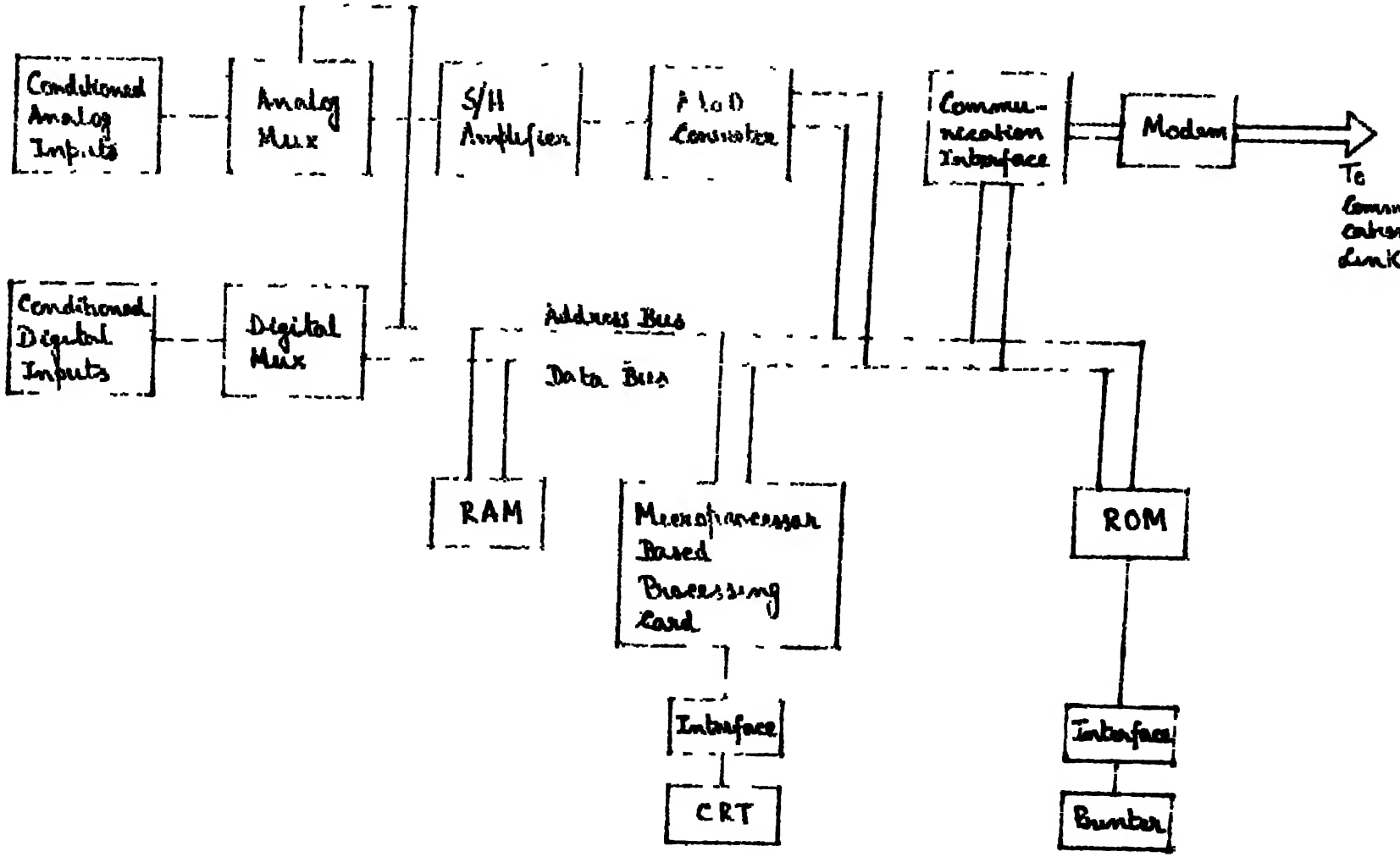

Conditioned Analog Inputs
Analog Mux
S/H Amplifier
A to D Converter
Communication Interface
Modem
To
Conditioned Digital Inputs
Digital Mux
Address Bus
Data Bus
RAM
Microprocessor Based Processing Card
ROM
Interface
CRT
Interface
Buzzer

Fig 26

- Controlling and display annunciator system for digital status changes and out of limit conditions of analog values.
- Supervision of communication channel and equipment status. Interfacing operator's Desk.

2.4 SCADA Software

The purpose of some of the important software packages are:

(a) To determine the validity of data

(b) To generate proper data base

(c) Generation of commands for supervisory control

(d) Message formating

(e) Updating the data base

(f) Diagnostic and corrective action

(g) Alarm indications

(h) Communication functions

(i) Logging of data

(j) Economic load despatch calculations, etc.

2.5 Scanning Methods

There are mainly four methods of scanning employed by the master station to obtain data from the slave station on the RTU. These are:

(a) Point-to-point Scan Method:

This is a simple system in configuration and requires one communication channel per remote station. The reliability is more in this case as each RTU is directly connected to the central unit through communication medium. However,this becomes costly when the number of remote stations is more.

(b) Time Slot Reporting Method:

This configuration is best suitable for both in expensive and high speed Multi-remote/Single Master SCADA system. Time Slot Reporting operates in the following manner. When a reporting sequence is to be started the master station sends a synchronising tone which all the remote stations hear. The RTUs synchronize their internal clocks (which are crystal controlled for high accuracy) at the end of the tone burst (trailing edge), and the time sequence then commences. The master station sends no further transmissions. Nothing happens during the first time slot which is called time slot zero. RTU No.1 will turn on and report its message during time slot number one. RTU No.2 will do the same during the time slot No.2, and this process will continue until all remotes have each reported back in their own time slot. This system requires a periodic

synchronisation from the master station which can be done on automatic bases in real time.

(c) Polling Method:

Time slot reporting is limited to only bringing data from the remote to the master station. Devices at the remote station cannot be controlled, nor can the master station lock to a specific remote station. Polling on the other hand, enables the master station to have full control over the TDM system as well as to control remote points. The remote station is first designed to perform the required reporting and the control functions as if it solely was to communicate with the master station in a one-to-one asis. The remote unit may perform simple functions or it may be highly complex select/check/operate configuration. Very simple logic is then added to the RTU design to adopt it for polling operation. The major part of this logic is an address comparator which detects if the address received from the master station corresponds to that RTU's address code. In this configuration actually the central unit contacts each RTU and asks for data. This method is best suited for cost effective telemetry and telecontrol system.

(d) Loop Scan Method:

This is best suited for a number of RTUs which are located in line geographically with respect to the central station. Communication channel saving and reduction in the central unit are the main criteria in selecting this method. All the remote stations are looped in this configuration and the data pertaining to all these remote stations are transmitted in a single communication channel. This is best suited for Power System Network where the number of communication channels are restricted. The remote stations will transmit data one after another with their address and the common central unit will receive the data and store it in the particular memory locations which is allotted for each RTU.

2.6 Scope of the Present Work

This includes the designing and implementation of a one-way link between a RTU and the central station. The RTU is designed as a data acquisition and transmission unit and the central station is designed to receive and display them. So the RTU is referred to as the Transmitter and the central station as the Receiver in the Thesis. The transmitter along with such other units are assumed to be connected with the receiver in a star configuration. The

scanning method employed for transfer of data from the transmitter to receiver is point-to-point scan method. Optical fibre is used as the communication link for reasons mentioned in the previous chapter.

CHAPTER 3

SYSTEM DESIGN

3.1 The overall design of the system will depend upon the nature of parameters we are going to monitor and the type of display we want. The parameters of interest are as follows:

1. Voltages 'V':

Voltages are of sinusoidal in nature at a frequency of 50 Hz. Magnitude of the voltages may vary from system to system. It may be of the order of Kilo volts e.g. 11 kV, 33 kV or even more for transmission lines. General purpose domestic lines have an r.m.s. voltage of 220 V. Also for a single phase system we have only one voltage to monitor, whereas for a three phase system, which is being considered here we have three voltages to monitor.

2. Currents 'I':

The currents are also sinusoidal in nature with a frequency of 50 Hz. Current is a highly variable factor. Voltages do not vary much for a system in normal conditions, but current magnitudes may vary even in normal conditions.

For a practical system it may range from a few amperes at no load to Kiloamperes at full load, e.g. transmission lines. So current is a load dependent factor. It increases drastically when fault occurs.

3. Phase Angle 'ϕ':

The phase angle which is defined as the time domain log or lad of the current waveform with respect to the voltage waveform is also an important parameter. It gives us an information about the nature of the load, and the power factor.

Total Power (or Apparent Power) = Real. Power + Reactive Power.

If $\bar{V}$ and $\bar{I}$ are the voltage and current vectors, respectively, where the current vector is leading the voltage vector by ϕ degrees

$$\bar{V} = V \quad 0 , \quad \bar{I} = I \quad \phi ,$$

$$\text{then Apparent Power} = \bar{V}^{*} \cdot \bar{I}$$

$$= V I \quad \phi$$

$$= V I \cos \phi + j V I \sin \phi$$

$$\therefore \text{Real Power} = VI \cos \phi$$

$$\text{Reactive Power} = VI \sin \phi$$

$$\text{Power Factor} = \frac{\text{Real Power}}{\text{Apparent Power}} = \cos \phi$$

So Cos ϕ gives a measure of the power factor.

The parameters of interest are elaborated in Fig.3.1.

3.2 In this section, we give a brief description of each of the three modules i.e. Transmitter, Optical-fibre Link and Receiver, that make up the system.

3.2.1 Transmitter

The transmitter unit consists of two blocks. One is a data acquisition block followed by a data processing and subsequent transmission block. This unit has also display facilities to flash the different parameters from time to time. Whenever a parameter is detected faulty by the transmitter it sends a message down the fibre-optic link to the receiver. The inputs to this unit are six sinusoidally varying voltage waveforms, three for the three phase voltages and three for the three phase currents (obtained by converting current waveforms into voltage waveforms by proper scaling), varying between 0 to $\pm$ 2 Volts in normal conditions. The actual voltages and currents of the system to be monitored is at a very high level. So they are stepped down by potential transformers (PT) and current transformer (CT) respectively. In this work we have not implemented these things and assume that their output is available to us.

The transmitter unit starts with an input protection and buffer block which isolates it from the PT and CT. Then we have a sample and hold block meant for sampling and holding

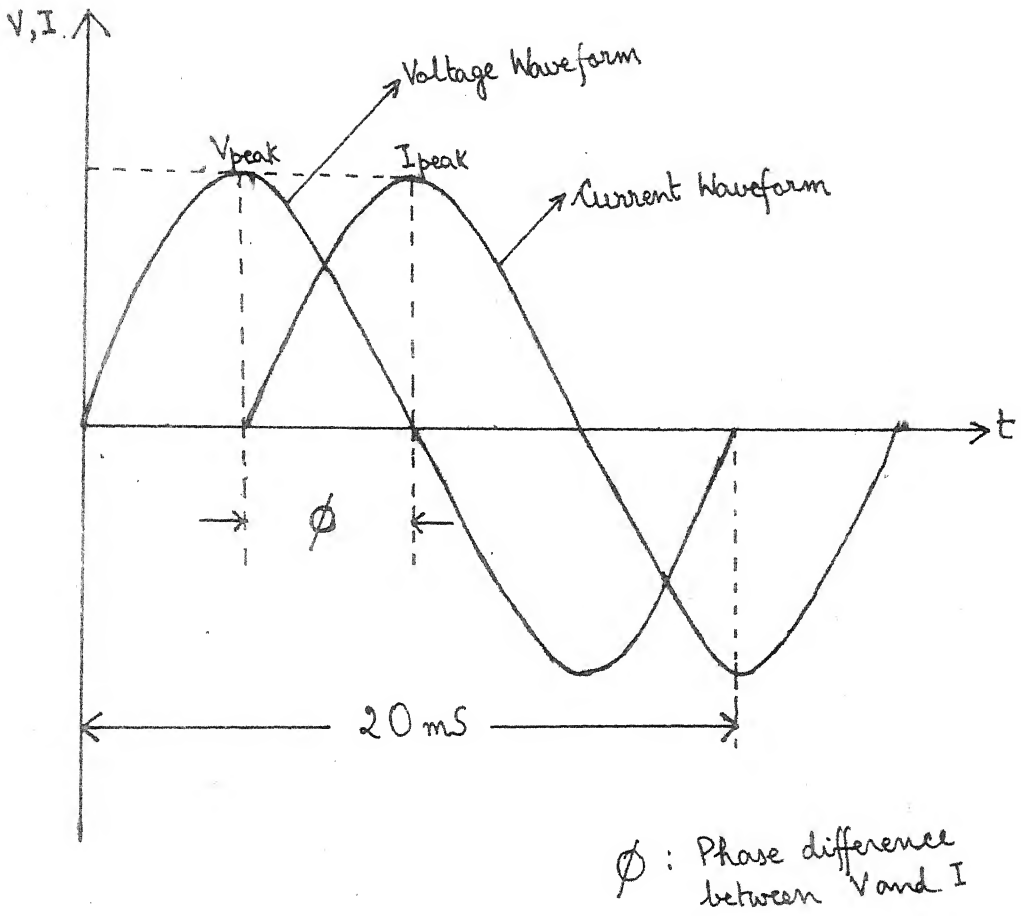

V, I
Voltage Waveform
Vpeak
Ipeak
Current Waveform
t
ϕ
20 mS
ϕ : Phase difference between V and I

Fig. 3.1

of the analog sinusoidal input. The switches of this block is controlled by a channel selector. The outputs of the sample and hold block is fed to a multiplexer which in turn feeds them one by one to the analog input of a analog-to-digital converter. The operation of the above mentioned blocks are controlled by a timing block. All these blocks make up the data acquisition part of the transmitter.

The data processing and subsequent transmission part of the transmitter has a 8085 chip used as the CPU. This controls various other blocks in this part of the transmitter such as RAM, EPROM, Programmable Peripherial Chip 8255, USART 8251 and Timer/Counter 8251 etc.

3.2.2 Fibre-Optic Link

The fibre optic link we are using/are devices made by Hewlett Packard. The link consists of three units - the transmitter, the optical fibre and the receiver. For the transmitter the HFBR-1001 fibre optic transmitter was used. This is an integrated electrical to optical transducer designed for digital data transmission over single fibre channels. A bipolar integrated circuit and GaAsP LED convert TTL level inputs to optical pulses at data rates from d.c. to 10 Mb/s NRZ. The HFBR-1001 is intended for use with HFBR-3000 fibre optic cable/connector assembles and the HFBR-2001 fibre optic receiver for transmission distances

upto 100 meters. The HFBR-1001 generates optical signals in either of two externally selectable modes. The internally coded mode produces a 3-level code optical signal for reception and decoding by the HFBR-2001 receiver. This feature provides data format independence over the data rate range of d.c. to 10 Mb/s NRZ while allowing for wide dynamic range and high sensitivity at the receiver. The externally-coded mode produces a 2-level optical signal which is a digital replica of the data input waveform. Used in this mode with the HFBR-2001 receiver the user must provide proper data formatting to ensure proper receiver operation. In our case we have used the former mode i.e. internally coded mode.

The HFBR-2001 fibre optic receiver is an integrated optical to electrical transducer designed for reception of digital data over single fibre channel. A silicon PIN photodetector and bipolar integrated circuit convert optical pulses to TTL level output with an optical sensitivity of 8.8 μW and data rates upto 10 Mb/s NRZ.

The optical fibre cable HFBR-3000 uses a single fused silica, partially graded index, glass-clad fibre surrounded by silicone coating, buffer jacket, and tensile strength members. This combination is then covered by a scuff- resistant outer jacket. The cable resistance to mechanical abuse, safety in flammable environments, and inherent

absence of electromagnetic effects may make the use of conduit unnecessary. However, the light weight and high strength of these assemblies allow them to be drawn through most electrical conduits.

3.2.3 Receiver

The receiver unit is so designed that it will scan a number of transmitters, for any message sent, one after another sequentially and then displays the message. Intel 8085 chip works as the CPU here. A USART 8251 is interfaced with it (for each transmitter) to completed the link between the transmitter and the receiver. The various other blocks in the receiver are RAM, EPROM, Timer/counter etc.

The system block diagram consisting of the above three units is given in Fig.3.2

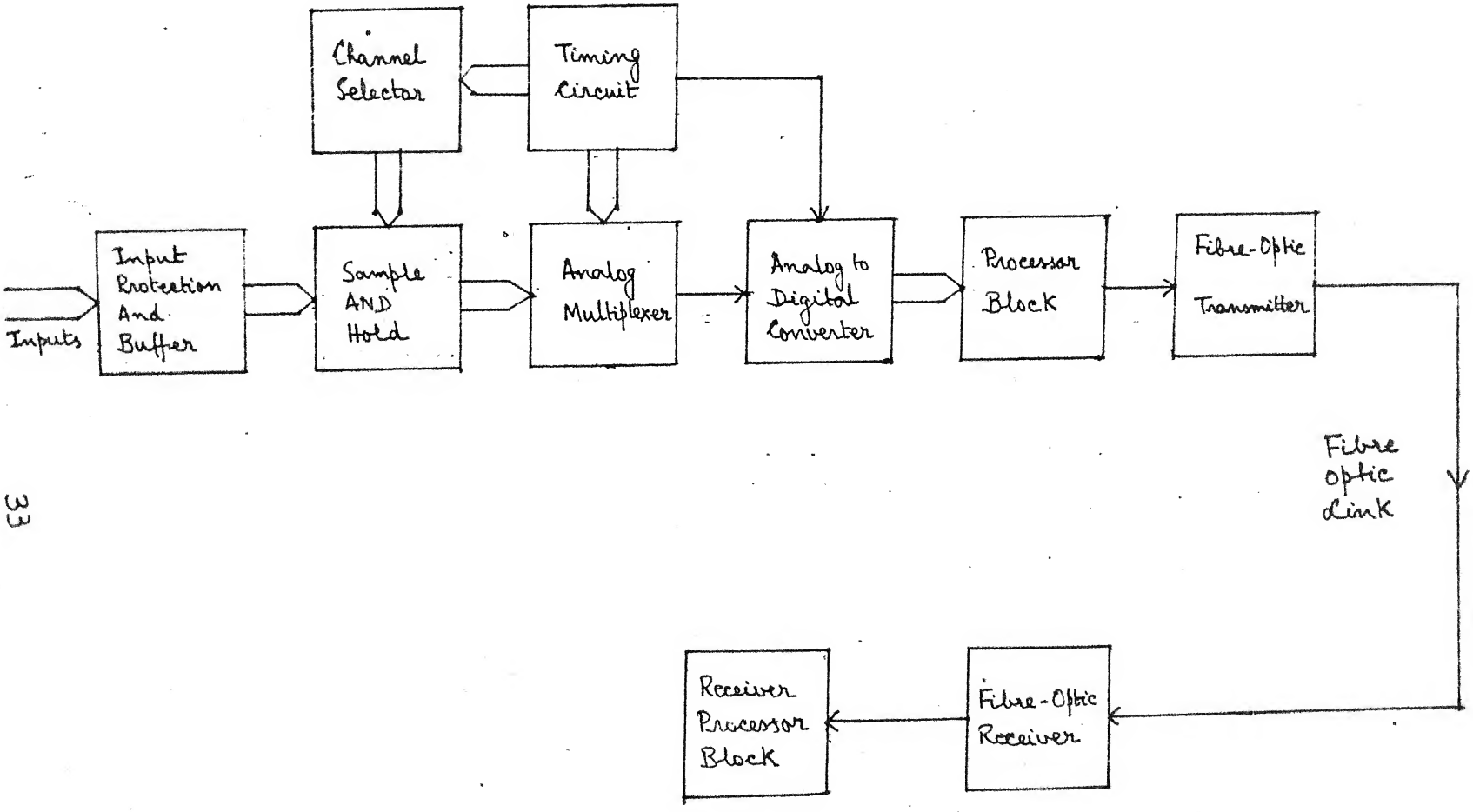

Channel Selector
Timing Circuit
Inputs
Input Protection And Buffer
Sample AND Hold
Analog Multiplexer
Analog to Digital Converter
Processor Block
Fibre-Optic Transmitter
Fibre optic Link
Receiver Processor Block
Fibre-Optic Receiver

Fig. 3.2.

CHAPTER 4

REALIZATION OF THE HARDWARE

4.1 Transmitter

The transmitter can be mainly divided into two basic blocks. One is the data acquisition block and the other one is the data processing and the transmission block. In the data acquisition block we have six sinusoid voltages representing the 3 phase voltages, Va, Vb, Vc and 3 phase currents Ia, Ib, Ic as the input. The voltage swing of each of these voltages in normal conditions is $\pm$ 2 volts and the voltages are adequately phase shifted from each other. However under abnormal conditions the voltage swings can go as high as $\pm$ 5 volts. The frequency of each of these voltages is 50 Hz, which is the line frequency.

4.2 Hardware Related to Data Acquisition

Now we have six voltages of varying phase and amplitude whose instantaneous values should be available to the data processing unit for required calculations as and when desired by it.

First of all we make sure that the data acquisition block is not affected if the output of the voltage and current transducers becomes many order higher than the normal

values due to some fault in the system. For such high inputs diode protection for each channel is provided right at the input followed by buffers.

Next to the buffers are the sample and hold (S/H) units. We have six channels and for each one S/H unit is required. So altogether we have six S/H units. The sampling rate is determined by the Timing circuit and is fixed at 8 KHz. This is so done as the output of the S/H circuits are fed to a analog multiplexer whose channels are selected by turn with a time gap corresponding to 1/8 KHz. So effectively we have at the output of the multiplexer sine waves which are sampled at a rate of 1 KHz. Since the frequency of each sine wave is 50 Hz so we have 20 samples for a period of each waveform. However there is flexibility to change the sampling rate at will as the output frequency of the timing circuit can be varied. The switches, of the S/H circuit, which allow the charging or discharging and holding of the S/H capacitor are activated by a channel selector which is nothing but a 3 to 8 decoder. It has got three input lines coming from the timing circuits and eight output lines. When a particular 3 bit pattern comes to the input lines the corresponding output line goes low, or else it remains high. The chip (NE 5537) we have used for the S/H circuit has an internal logic built in which takes the S/H output in the hold state when the logic

input of the chip is low, and when it is high the S/H circuit is in the sampling or tracking mode. The six S/H outputs are connected to the six inputs of a 8-channel multiplexer, the other two inputs being grounded. The channel selection logic of the multiplexer is same as that of the 3 to 8 decoder, so that when the output of a S/H of a channel goes into hold state that particular channel gets selected in the Mux and the value appears at the output. The output of the Mux is in turn connected to the analog input of the Analog-to-Digital converter (ADC) which converts the Mux analog output into digital form. The ADC output is interfaced to the µp via a 8255 for subsequent processing of the data. The chip select of the ADC is fixed at 8 KHz so that it can get hold of all the multiplexed values that are being fed at its input.

4.3 Timing Circuit:

The timing circuit consists of an astable multivibrator and counters. First of all a frequency of 32 KHz is generated using the 555 Timer in the astable mode. Then this frequency is divided by four to obtain a square-wave of 8 KHz which acts as the chip select of the ADC. This square wave is again divided by 8 with help of three flip-flops the outputs of each being fed to the corresponding channel-selector inputs of the 3-8 decoder and the Mux. These

outputs are also taken to the µp (8085) via an input part of 8255 so that the µp can know which channel is selected at any particular instant of time. The various waveforms generated is explained below in detail.

Clock : This is the 32 KHz main clock generated by the 555 Timer.

$\overline{CS}$ADC : Chip select of ADC obtained by dividing the clock by 4.

A : LSB of the logic for the channel selection of the Mux and 3 to 8 decoder. Obtained by dividing $\overline{CS}$ADC by 2.

B : Second bit of the logic for the channel selection of the Mux and the 3 to 8 decoder. Obtained by dividing A by 2.

C : MSB of the logic for the channel selection of the Mux and the 3 to 8 decoder obtained by dividing B by 2.

O/P0 to O/P7: These are the outputs of the 3 to 8 decoder corresponding to the three logic inputs ABC, i.e. when CBA = 000, O/P 0 = 0 and O/P 1 to O/P 7 = 1; when CBA = 001, O/P 1 = 0 and O/P 0, O/P 2 to O/P 7 = 1; and so on. These outputs are connected to the logic input of the S/H block for proper sampling and holding.

CS Mux 0 to CS Mux 7 : These waveforms are not actually generated but are given here to have a proper idea about the functioning of the circuit. Corresponding to the three logic inputs A,B,C to the Mux one of the channels is turned on, i.e. when CBA = 000, CS MUX 0 = 1 and CS MUX 1 to CS MUX 7 = 0. Similarly when CBA = 001, CS MUX 1 = 1 and CS MUX 0, CS MUX 2 - CS MUX 7 = 0 and so on.

A complete circuit of the Data Acquisition part of the Transmitter is shown in Fig.4.1. The various waveforms related to the functioning of the circuit is shown in Fig.4.2.

4.4 Principle of Working of the S/H Block

As mentioned earlier, have used NE 5537 chip for the S/H purpose. The basic concept of the S/H circuit incorporates the use of two operational amplifiers and a switch control mechanism, which determines sample, hold or track conditions. The block diagram of the NE 5537, given in Fig.4.3, is a closed loop non-inverting unity gain sample and hold system. The input buffer amplifier supplies the current necessary to charge the hold capacitor, while the output buffer amplifier closes the loop so that the output voltage is identical to the input voltage with

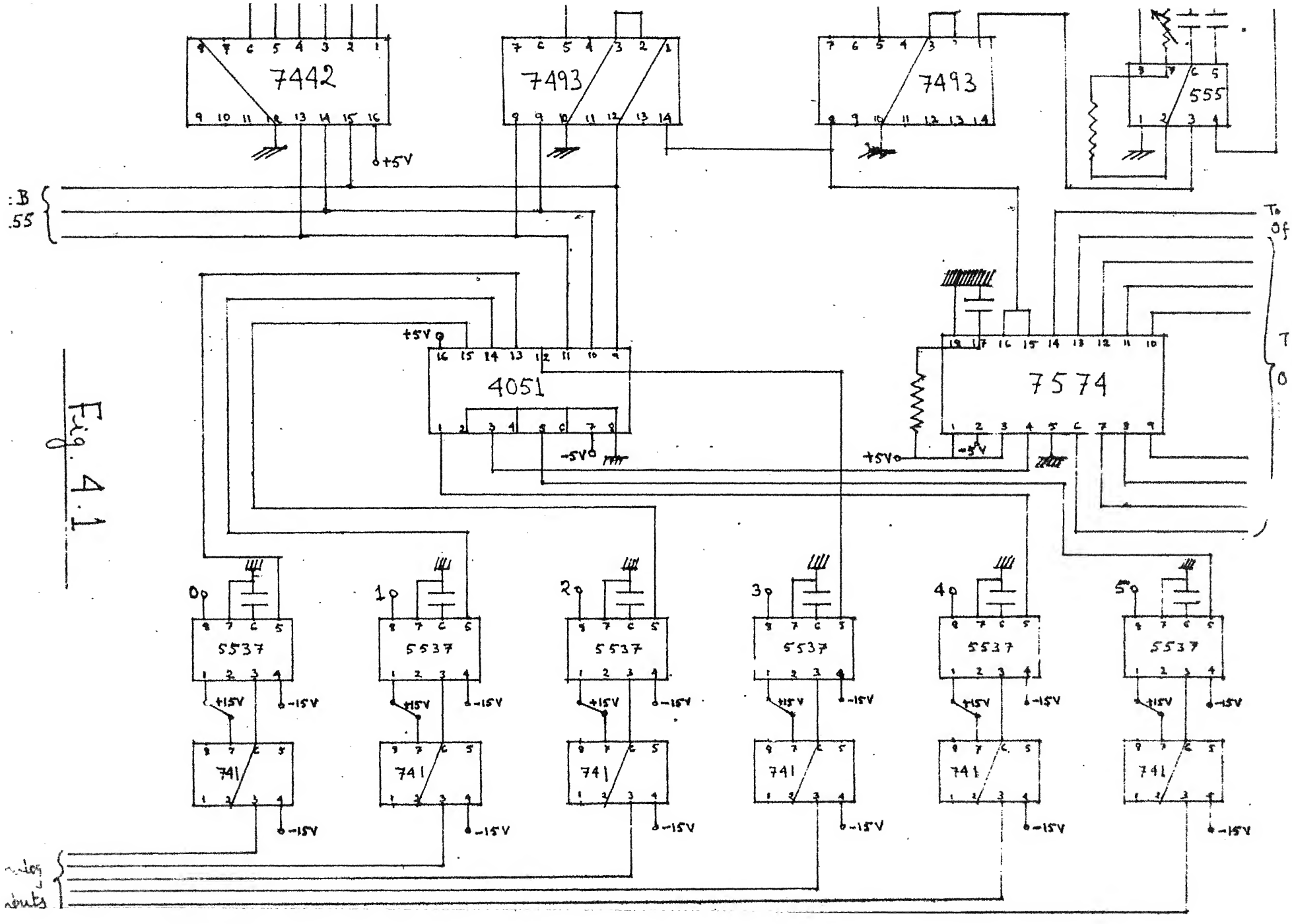
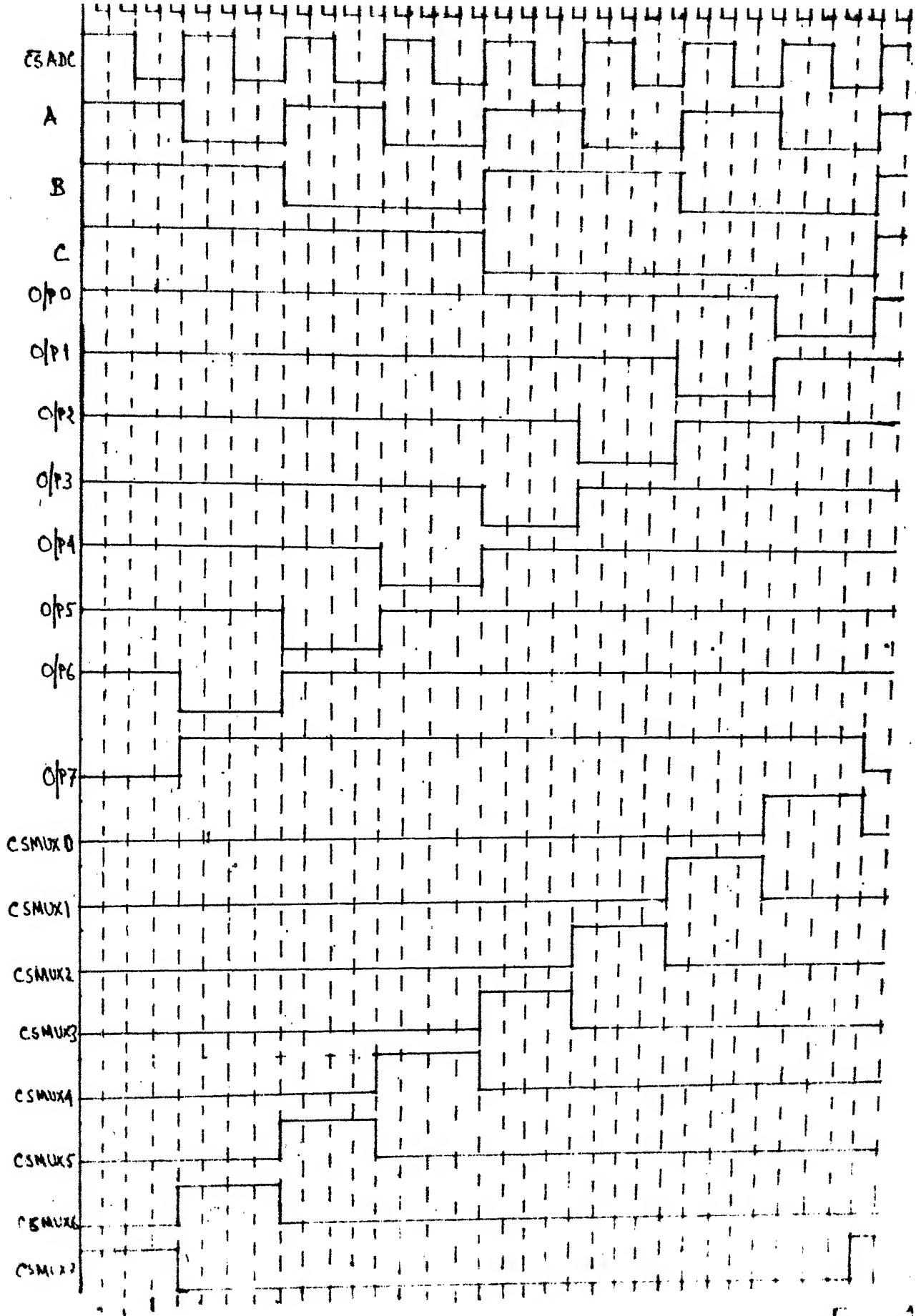

7442
7493
7493
555
4051
7574
5537
741
+5V
-5V
+15V
-15V
To
of
T
O
0
1
2
3
4
5

Fig. 4.1


$\overline{CS}$ ADC
A
B
C
O/P 0
O/P 1
O/P 2
O/P 3
O/P 4
O/P 5
O/P 6
O/P 7
CSMUX 0
CSMUX 1
CSMUX 2
CSMUX 3
CSMUX 4
CSMUX 5
CSMUX 6
CSMUX 7

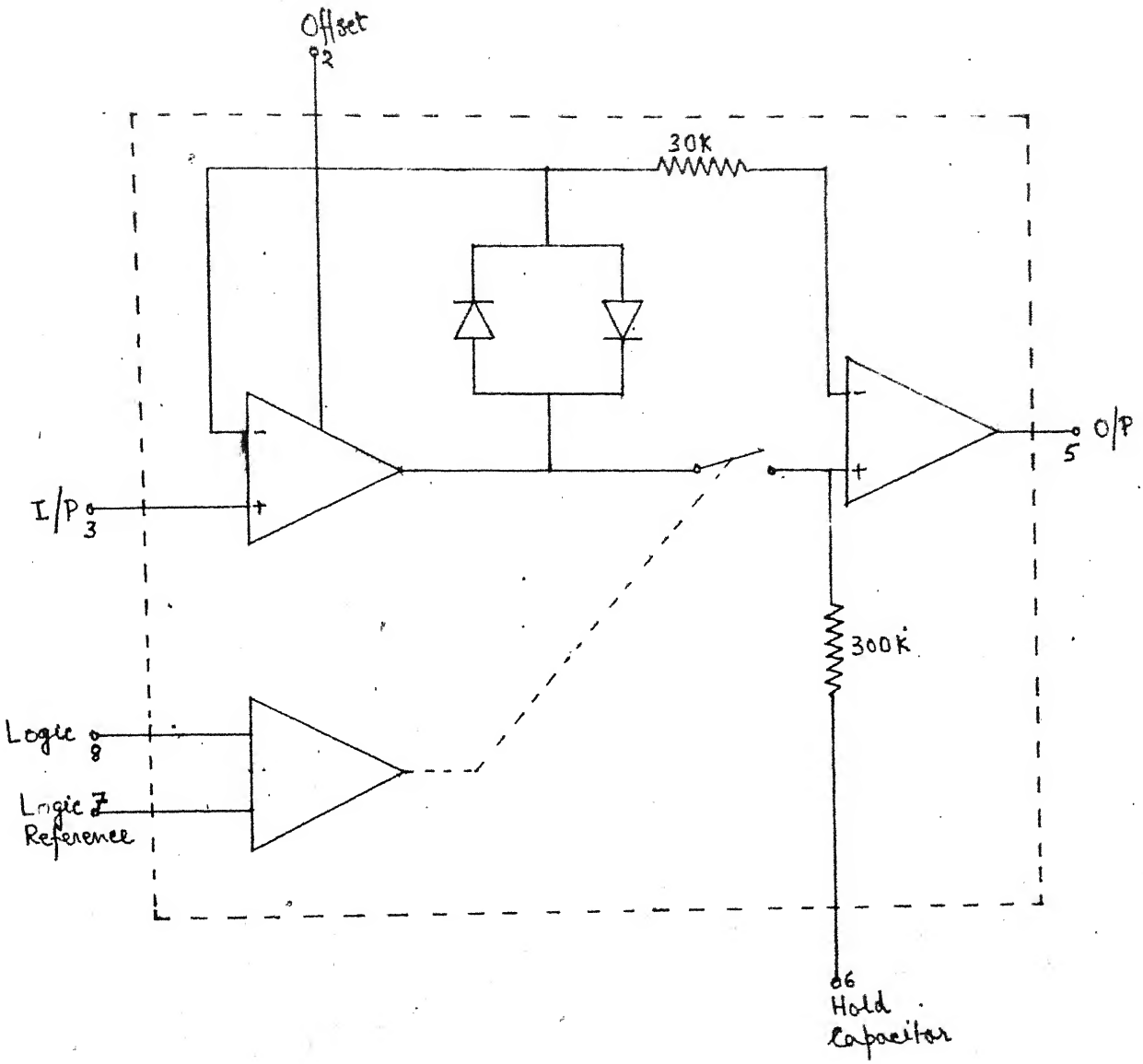

Offset
2
30K
I/P
3
O/P
5
300K
Logic
8
Logic
Reference
7
6
Hold
Capacitor

Fig. 4.3

considerations for input offset voltage, offset current and temperature variations which are common to all sample and hold circuits, be they monolithic, hybrid or modular.

When the sampling switch is open (in the hold mode) the clamping diodes close the loop around the input amplifier to keep it from being overdriven into saturation.

The switch control is driven by external logic levels, in our case the output of the 3 to 8 decoder. The switch control has a floating reference (pin 7), referred to as the logic reference which makes the sample and hold device compatible to several types of external logic signals (TTL, PMOS, and CMOS). The switching device operates at a threshold level of 1.4 V.

The switch mechanism is on (sampling an information stream) when the logic level is high and presents a load of 5 A to the input logic signal. The analog sampled signal is amplified, stored in the external holding capacitor and buffered. At the end of the sampling period, the internal switch mechanism turns off (switch opens) and the 'stored analog memory' information on the external capacitor (pin 6) is loaded down by an operational amplifier connected in the unity gain non-inverting configuration. The amplifier input impedance is given by

$$R = R_{IN} (A_{OL})/(1 + 1/A)$$

where,

R = Effective input impedance

R_{IN} = Open-loop input impedance

A_{OL} = Open-loop gain

A = AC loop gain

Therefore, the higher the open loop gain of the second operational amplifier, the larger the effective loading on the capacitor. The larger the load, the lower the leakage current and the better the droop characteristics.

Sampling time for the NE 5537 is less than 10 μsec. Leakage current is 6 pA at a rate output load of 2Kohms.

Since drive current of the input buffer of the S/H unit is finite and the leakage current in hold is not zero, the external capacitance, if large, limits the slowing rate in sample mode, and if small, converts leakage current droop in hold mode. The performance of a general S/H amplifier is given in Appendix A.

4.5 Principles of Working of the ADC

We are using AD 7574 as the ADC. It is a low cost 8 bit microprocessor compatible ADC which utilises the successive approximation technique to provide a conversion time of 15 μs.

The ADC is interfaced with the microprocessor in Slow-Memory Interface Mode. The timing diagram and the truth table

corresponding to this mode is given in Fig.4.4 and Table 4.1 respectively.

The operation of the ADC is Bipolar (Offset Binary) operation.

The details regarding this chip can be had from Data-Acquisition Databook of Analog Devices.

4.6 Selection of Components

1. Buffers:

   For this μ A 741 was chosen since it has high input differential voltage capacity = ± 15 V, apart from its other characteristics like high input impedance, low output impedance etc.

2. Channel Selector or 3 to 8 Decoder:

   For this actually a 4 to 10 decoder 7442 was used with its MSB logic input grounded so as to obtain a 3 to 8 decoder. This was so done as the 3 to 8 decoder chip was not available.

3. Sample and Hold:

   NE 5537 was chosen as the S/H amplifier. This amplifier has high accuracy, fast acquisition time and low droop rate.

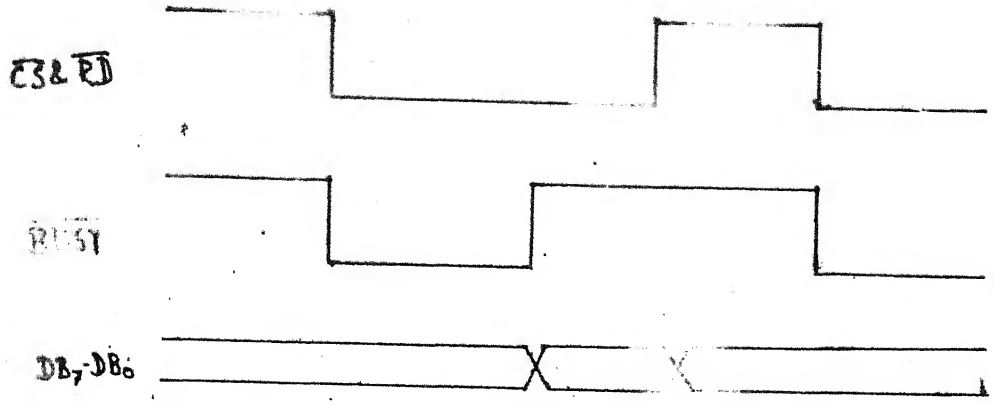


Fig. 4.4

AD7574 I/Ps	AD7574 O/Ps		AD 7574 Operation
$\overline{CS}$ & $\overline{RD}$	$\overline{BUSY}$	$DB_7 - DB_0$	
H	H	High Z	Not Selected
H → L	H → L	High Z	Start Conversion
L	L	High Z	Conversion in Progress
L	L → H	High Z → Data	Conversion Complete
L → H	H	Data → High Z	Converter Reset
H	H	High Z	Not Selected

Table 4.1

4. Multiplier:

CD 4051 was used as the 8-channel analog multiplexer. The control input of this IC is compatible with T.T.L. levels. CD 4051 can take ± 5 V input voltage and hence is fit for the circuit.

5. Clock:

NE 555 (Timer) was used as clock as it has reasonably high temperature stability and is TTL compatible. The important feature to be noted here is that 555, unlike many RC timers provide a timed interval that is virtually independent of supply voltage V_{cc}.

6. Counters:

Two 7493 chips were used. Each one has four flip-flops so division by 2 upto 16 is obtainable by properly setting the reset pins whenever it is needed.

7. Analog to Digital Converter:

AD 7574 was used for this purpose. It has a moderately high conversion time of 15 μ s. The input voltage range it can handle is sufficient for our purpose.

4.7 Hardware related to Data Processing and Transmission

Once the sine waves of the different channels are converted into digital form, it is now the work of the μp to get hold of this digital data and check whether they are within the set limits or not, and if they are crossing these limits then the μp should send error messages via the USART 8251, which is connected to the fibre optic transmitter module, so that these error codes get transmitted to the receiving end. For this purpose a μp kit EC - 85 (manufactured by PEP) was used. A brief description of this kit is given in Appendix B. The kit is based on Intel 8C85 chip.

A 8255 chip was the input port. The three inputs we are interested in are (i) 8 bit data output of the ADC, (ii) the $\overline{\text{BUSY}}$ output of the ADC indicating start and end of conversion and (iii) The channel selection logic A,B,C, coming out from the timing circuits, to know to which channel the ADC output correspond. The 8-bit ADC data output was connected to port A of the 8255 which has the address 00. The $\overline{\text{BUSY}}$ line was connected to the LSB of port C whose address is 02. The three channel selection logic lines were connected 0th, Ist and 2nd bit of port B having an address 01. The control port of the 8255 has an address 03.

The 8251 is the output peripherial chip used for serial transmission of data. This was not available in the Kit and hence was externally interfaced. Its clock is the same as the system clock which is 2 MHz. The chip select of the 8251 for the control and data ports was generated by using a 4 input Nand gate. Threefore the inputs of the Nand gate came from address line A_7, A_6 and A_5 and the other input was connected to the IO/$\bar{M}$ line of p. The C/$\bar{D}$ line of the 8251 was connected to the address line Ao. Thus the control port address of the 8251 is E 1 and that of the data port is F0. These addresses were found alright as they did not clash with any other I/O address of the system.

The transmit clock (TxC) of the 8251 is obtained by dividing the system clock by 16 with the help of counter 1 of 8253 timer counter. This was so done as the clock for internal timing of the 8251 chip should be at least 13 times greater than Txc for it to operate in the asynchronous mode. Since we want to operate the USART in the asynchronous mode we divided the system clock by 16 to obtain a data transmission rate of 125 KHz. The output of the 8253 counter 1 was connected to the Txc input of 8251. The 8253 has the following addresses for the three counters and the control word. Counter 0 has address 10, counter 1 has 11, counter 2 has 12 and that of the control word is 13.

The clock of the counter 1 is connected to the 2 MHz system clock. Counter 1 is operated in Mode 3 with $N = (10)_H$ so as to obtain an output at 125 KHz which is connected to the Txc of the 8251. However setting $N = (0D)_H$ we can obtain the maximum data transmission rate with the present system which will be around 150 KHz.

A block schematic of the data processing and subsequent transmission of it is given in Fig.4.5.

4.8 Receiver

The hardware of the receiver is very much the same as that of the data processing part of the transmitter. Here also we have another PEP EC-85 Kit with Intel's 8085 chip as the microprocessor. In the receiver, the 8251 is connected in the receiving mode and 8255 is not needed. The Rxc (Receive Clock) of the USART is obtained in the same way as described in the transmitter above and is fixed at 125 KHz. The $\overline{CS}$ and $C/\overline{D}$ of the 8251 is also generated in the same way. A block schematic of the receiver hardware unit is given in Fig.4.6.

In both transmitter and the receiver, the display facilities available with the EC-85 Kit was used to display various quantities like voltage and current peak and r.m.s. values, power factor, power etc. in the transmitter and the error messages in the Receiver.

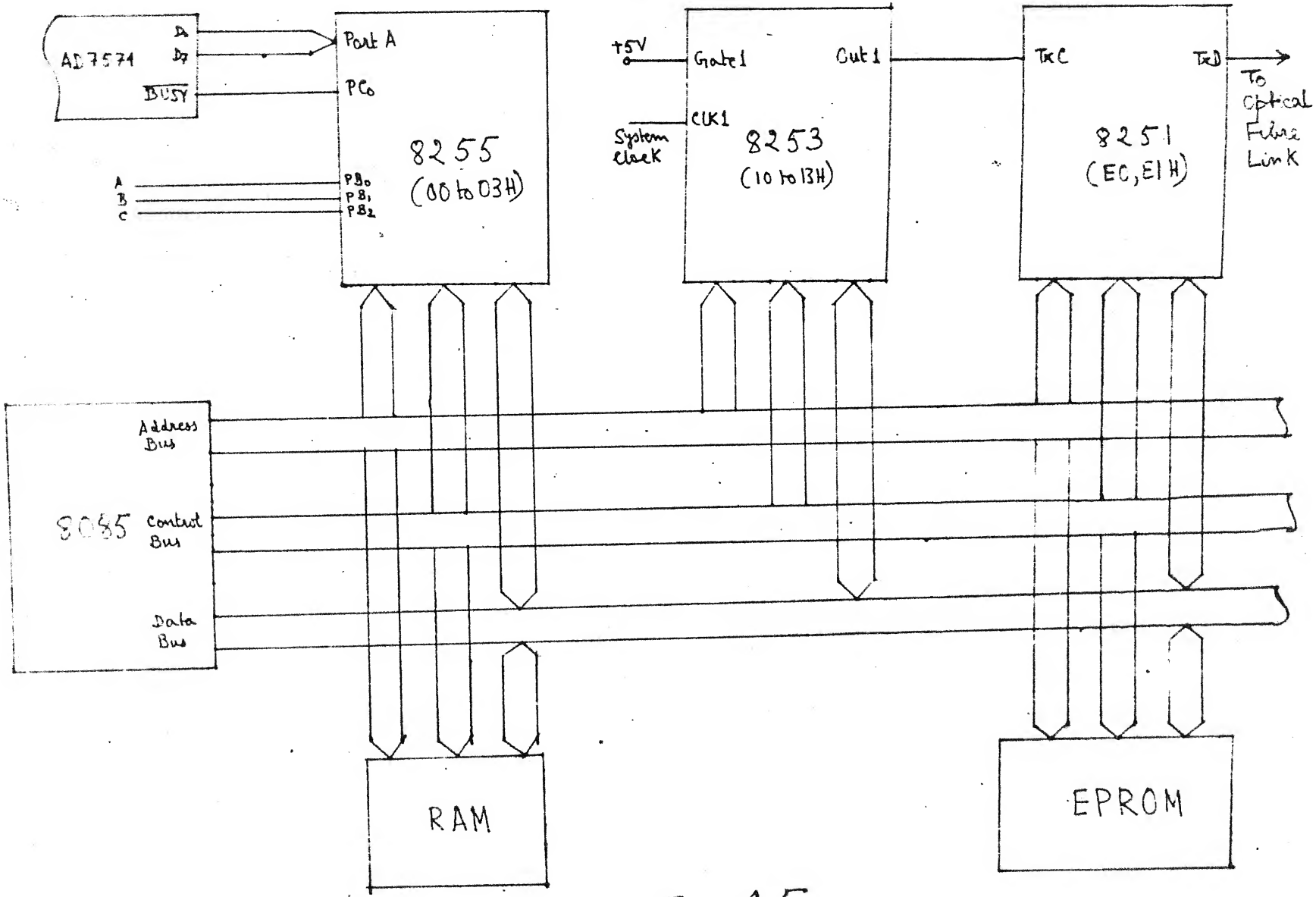

AD7571
D6
D7
BUSY
Port A
PC0
8255
(00 to 03H)
A
B
C
PB0
PB1
PB2
+5V
Gate 1
Out 1
CLK1
System clock
8253
(10 to 13H)
TxC
TxD
To Optical Fibre Link
8251
(EC, E1H)
Address Bus
8085
Control Bus
Data Bus
RAM
EPROM

Fig. 4.5

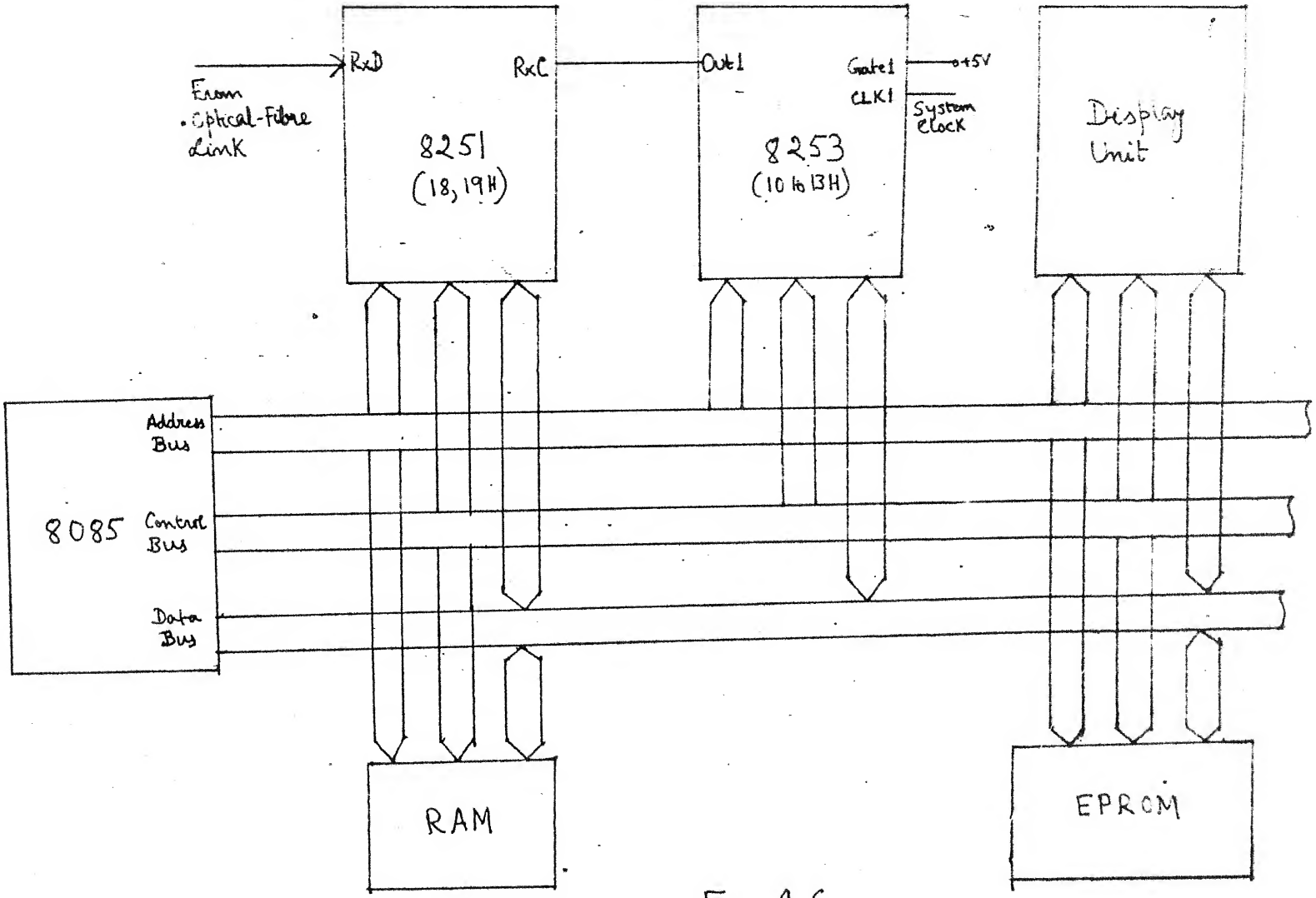

From
Optical-Fibre
Link
RxD
RxC
8251
(18, 19H)
Out1
Gate1
CLK1
+5V
System
Clock
8253
(10 to 13H)
Display
Unit
8085
Address
Bus
Control
Bus
Data
Bus
RAM
EPROM

Fig. 4.6

CHAPTER 5

SYSTEM SOFTWARE DESIGN

5.1 Transmitter

For writing the software of the transmitter, the following steps should be kept in mind.

1. Initialisation:

   Here the 8255 ports, A,B,C are programmed in the input mode, the 8251 is programmed in the asynchronous mode for data transmission and the counter 1 of 8253 is programmed in mode 3.

2. The 3 phase voltages Va, Vb, Vc are in channels 0, 2 and 4 and the 3 phase currents Ia, Ib, Ic are in channels 1,3 and 5, respectively. A particular channel corresponding to a particular phase voltage is chosen.

3. The peak and r.m.s. value of this voltage is determined by the μp. If these values are found to cross some set limits then an error message is transmitted through the 8251. For example in normal conditions we are supposed to have sine waves having ± 2 volts voltage excursions. On obtaining the peak (position) we compare the value with ADC outputs corresponding to + 2.5 volts, +1.5 volts and +4.5 volts. If it is above the first limit and below the third limit then we declare an

over voltage or over current condition has appeared. If it is below the second limit then we declare a under voltage or under current condition has appeared. Lastly if the value is greater than the third limit then a surge condition is declared.

4. If the peak voltage of a particular phase is found to be within the limits, its value is stored. Next we select a channel which contains the current information of the same phase. Its peak and r.m.s. values are determined and it is ensured that they are within the set limits, otherwise error signals are sent via the 8251. The phase angle difference between the voltage and current is also obtained by properly activating a counter.

5. The above steps are carried out for the other two phases also.

6. Once we know V_{peak}, $V_{r.m.s.}$, I_{peak}, $I_{r.m.s.}$ and phase angle and (ϕ), the power factor, real power, reactive power etc. are easily calculated.

5.2 Processing of V, I and ϕ in General

The following steps should be followed for processing V, I and ϕ.

1. We take a phase voltage (say Va) and call it Va_{prev2}. Then a next sample value of Va is taken and is called $Va_{prev.1}$. These two are stored in two memory locations. Similarly we take two successive samples of I_a and store them in two memory locations, calling the first one I_{prev2} and the second one Ia_{prev1}. These values of V_a and I_a are stored far comparison purposes.

2. Next a value of V_a is taken and is called Va_{new}. This Va_{new} is compared with Va_{prev1}. If found greater, this means that the waveform is rising so we replace so we replace $Va_{prev\ 1}$ by Va_{new} and $Va_{prev\ 2}$ by $Va_{prev\ 1}$. But if Va_{new} is less than $Va_{prev.1}$ we go back and check if $Va_{prev\ 1}$ is greater than Va_{prev2}. If it is so then Va_{peak} has occurred and is equal to Va prev.1. So we multiply by a constant to obtain $Va_{r.m.s.}$.

3. At the same time we start detection of Ia_{peak} and start a counter to upcount, which stops when Ia_{peak} has occurred. Ia_{peak} is also obtained in a similar manner as stated in step 2 above. From Ia_{peak} we get $Ia_{r.m.s.}$. The counter is stopped and its value is multiplied by a constant to give the phase angle ϕ_a. ϕ_a is obtained on the basis that the counter is counting the number of Ia samples between Va_{peak} and Ia_{peak}.

The flow-chart for obtaining peak and r.m.s. values of Va and Ia and the phase angle ϕ is given in Fig.5.1.

Two things should be noted here—

(a) We are detecting Va peak first, and we are not processing Ia information till the Va_{peak} occurs. So we are computing the lag of Ia with respect to Va.

(b) We are doing comparisons only for the quantities in the positive half cycle.

In a similar format we compute the other two sets i.e. V_b, I_b, ϕ_b and V_c, I_c, ϕ_c.

A complete flow chart for the development of the software is given in Fig.5.2.

An assembly language program was developed and its complete listing is given in Appendix C.

Receiver

The Receiver Unit is basically a display unit. The receiver gets hold of the error messages sent by the transmitter and displays it so that one can know where the fault has occurred. One thing should be kept in mind that although in the present system we have a single transmitter, in actual systems there will be several transmitters and the Receiver should be able to cater to all the

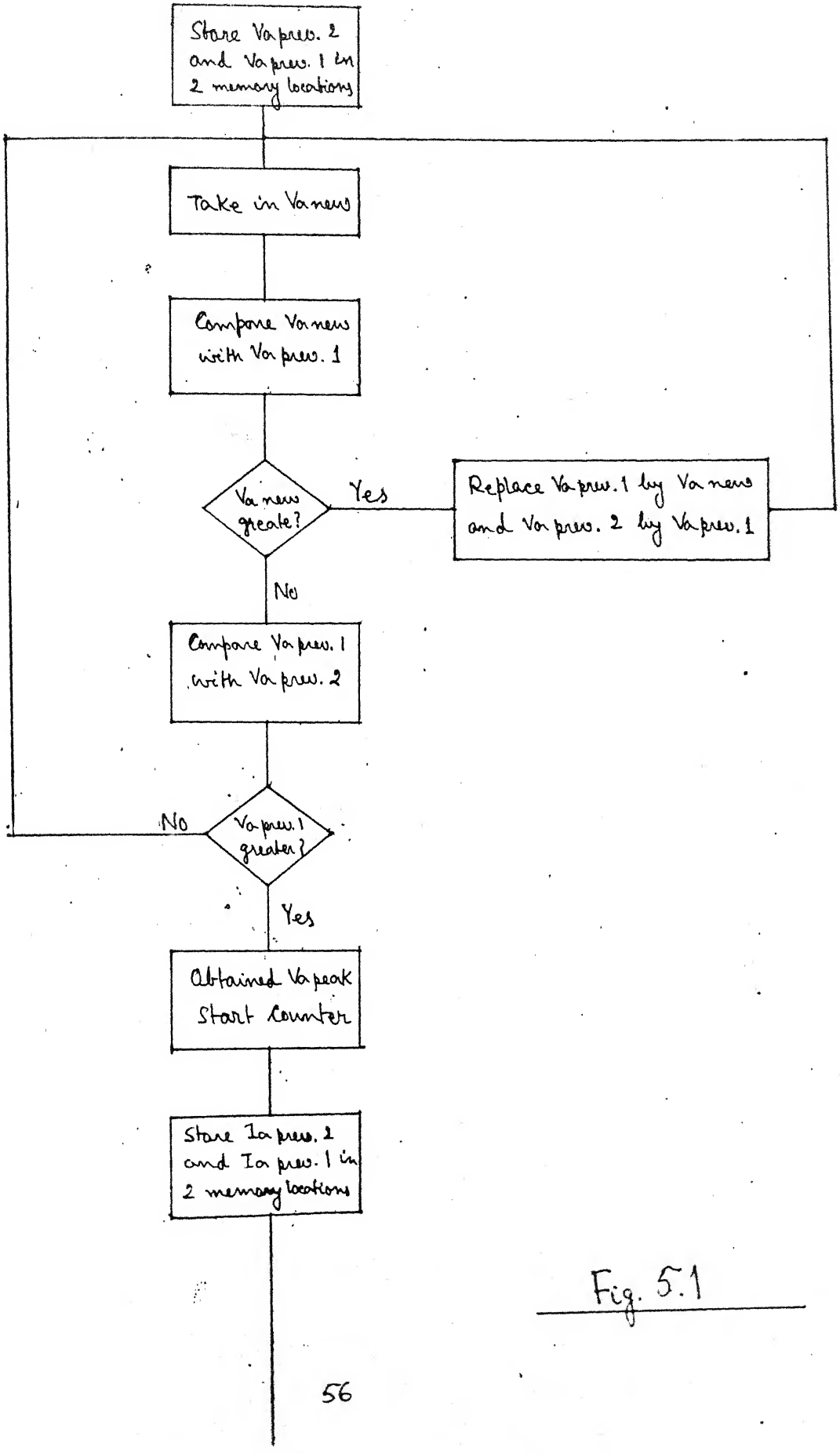

Store Va prev. 2 and Va prev. 1 in 2 memory locations
Take in Va new
Compare Va new with Va prev. 1
Va new greate?
Yes
Replace Va prev. 1 by Va new and Va prev. 2 by Va prev. 1
No
Compare Va prev. 1 with Va prev. 2
No
Va prev. 1 greater?
Yes
Obtained Va peak Start Counter
Store Ia prev. 2 and Ia prev. 1 in 2 memory locations

Fig. 5.1

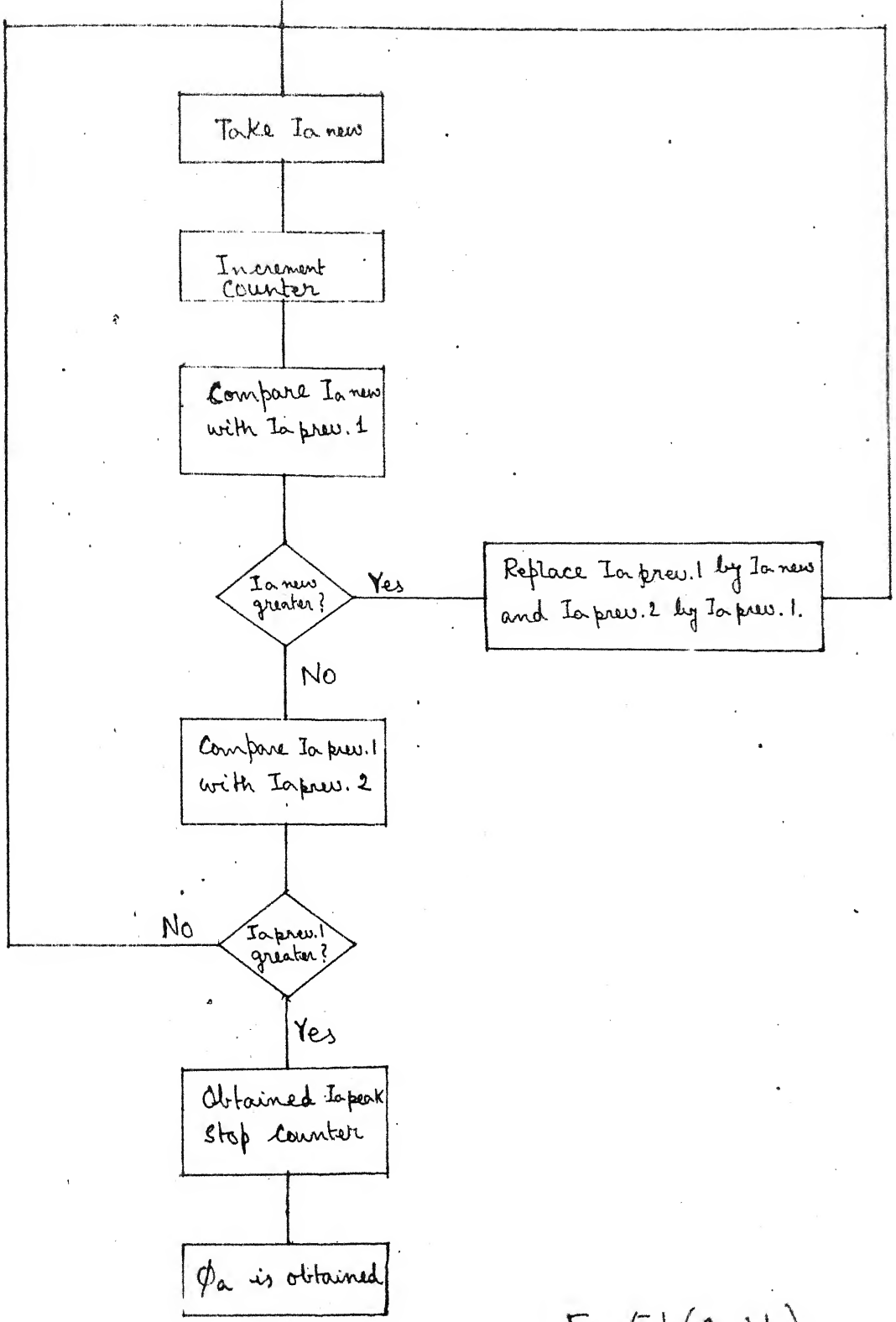

Take Ia new
Increment counter
Compare Ia new with Ia prev. 1
Ia new greater?
Yes
Replace Ia prev.1 by Ia new and Ia prev.2 by Ia prev. 1.
No
Compare Ia prev.1 with Ia prev. 2
No
Ia prev.1 greater?
Yes
Obtained Ia peak Stop Counter
ϕ_a is obtained

Fig 5.1 (Contd.)

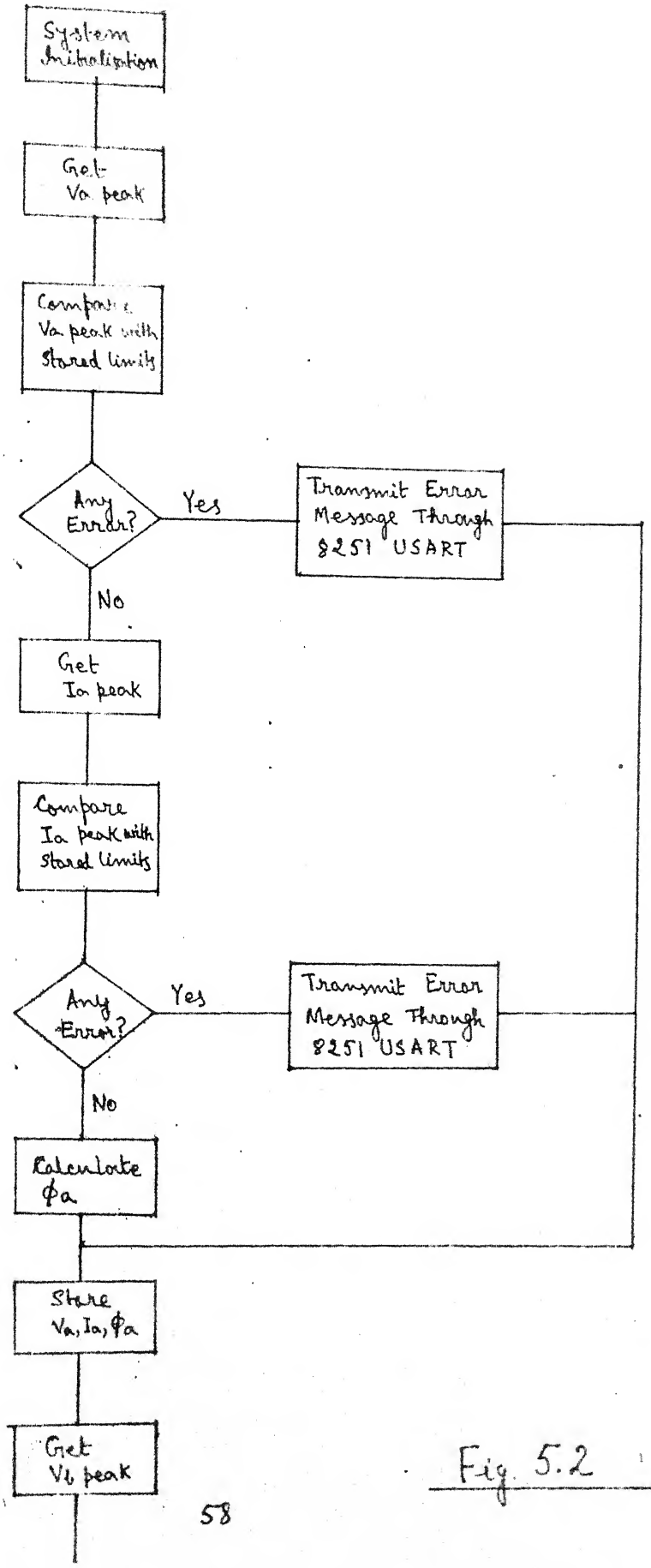

System Initialization
Get Va peak
Compare Va peak with Stored limits
Any Error?
Yes
Transmit Error Message Through 8251 USART
No
Get Ia peak
Compare Ia peak with Stored limits
Any Error?
Yes
Transmit Error Message Through 8251 USART
No
Calculate ϕa
Store Va, Ia, ϕa
Get Vb peak

Fig. 5.2

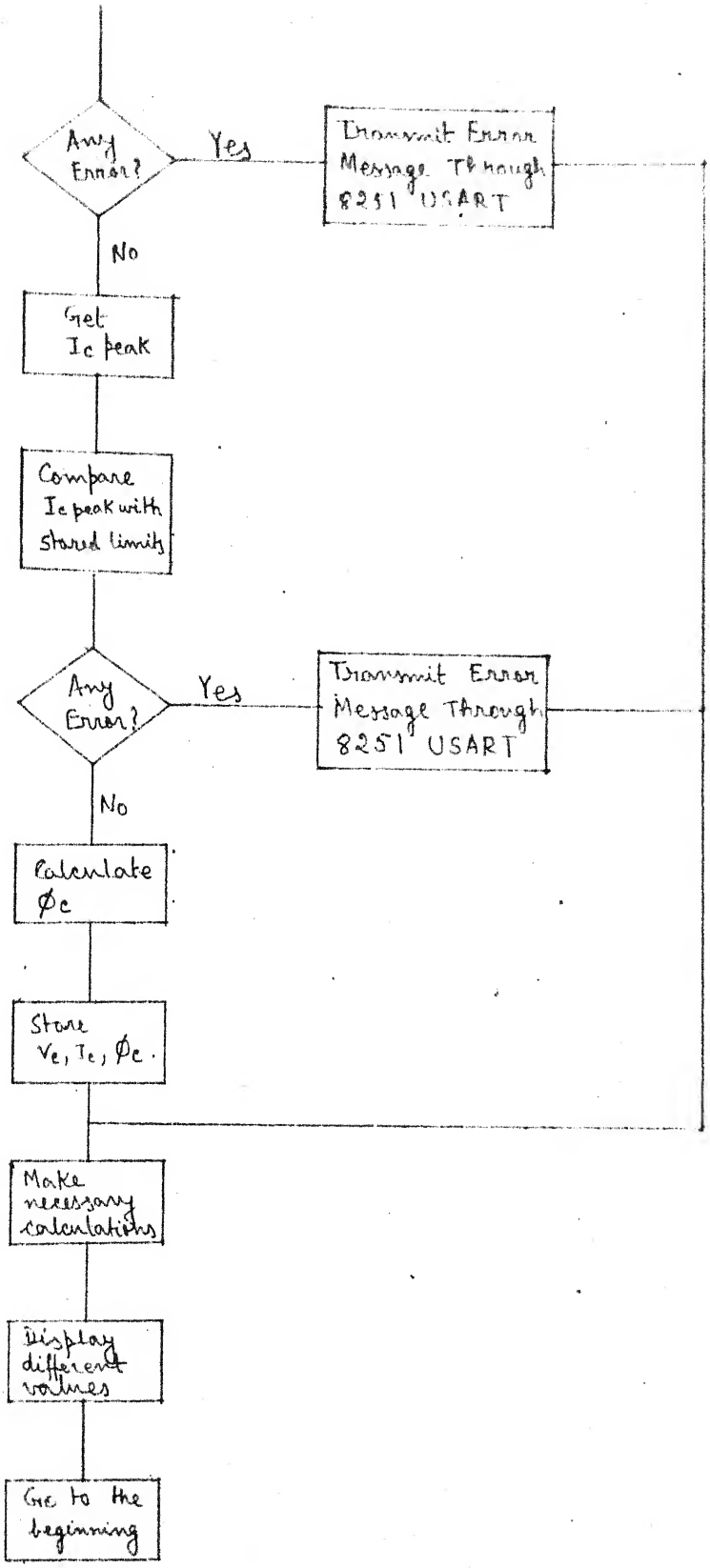

Any Error?
Yes
Transmit Error Message Through 8251 USART
No
Get Ic peak
Compare Ic peak with stored limits
Any Error?
Yes
Transmit Error Message Through 8251 USART
No
Calculate Øc
Store Ve, Ie, Øc.
Make necessary calculations
Display different values
Go to the beginning

Fig 3.2 (contd)

Transmitters. To be able to do this the Receiver CPU accesses the 8251s connected to the different transmitters in a Time-Division.- Multiplexed mode. That is it checks each USART for data in a cyclic way. The CPU check the R_x RDY bit of the 8251 status byte which is connected to say Transmitter 1. If it is set then data (i.e. error message) is there and CPU reads and displays it. If it is reset there is no error message till now and the CPU shifts its controls to the next 8251 which is connected to Transmitter 2 and the same process is carried out.

The USART 8251 in the Receiver is programmed in the asynchronous mode for receiving data. The 8253 counter 1 is programmed in mode 3 to generate the Rxc of the 8251.

A complete flow-chart for the receiver software is given in Fig.5.3. The Assembly Language Program is given in Appendix C.

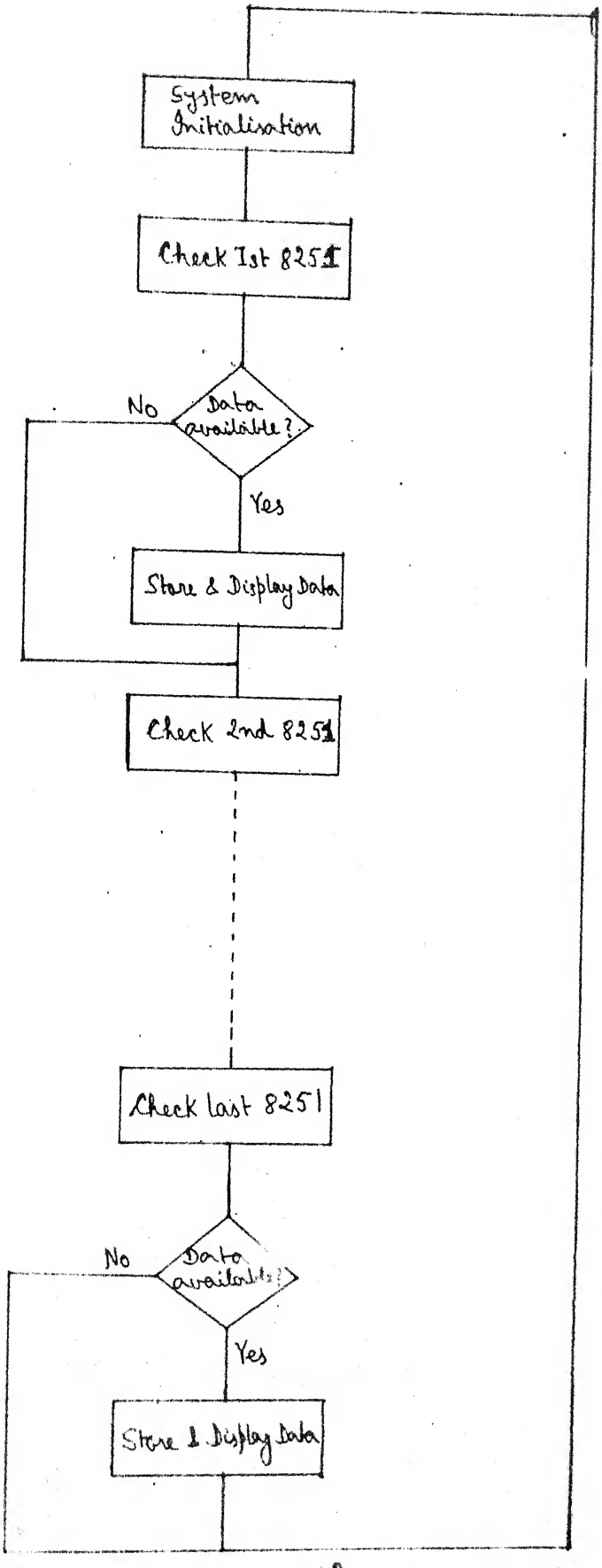

System Initialisation
Check 1st 8251
No
Data available?
Yes
Store & Display Data
Check 2nd 8251
Check last 8251
No
Data available?
Yes
Store & Display Data

Fig. 5.3

CHAPTER 6

CONCLUSION

Having thus designed and implemented the Transmitter and the Receiver for the purpose of telemetry in Power Systems, in this chapter, we will try to evaluate the performance of the system in terms of its capabilities and try to give some suggestions as to how this can be enhanced.

As mentioned in Chapter 1, the main parameters of interest in such applications are -

(i) Analog Parameters:

Line or phase voltage

Line or phase current

Power flow, MW

Reactive power flow, MVAR

Power factor

Energy

Line Frequency

(ii) Digital Parameters:

Circuit breaker status

Isolator status position

Transformer tap position

Alarms.

The classification of analog and digital parameters is made on the basis of the nature of the input to the data acquisition system of the transmitter. Thus where the inputs are analog we call the corresponding parameters as analog parameters and for digital inputs the parameters are called digital parameters.

As is clear from the discussions in the previous chapters, we have taken care of the analog parameters with the exception of line frequency. The line frequency can be easily determined using the software by detecting successive zero-crossings of a waveform and noting the time interval between them with a counter suitably clocked by a known frequency and calculating the average time period.

The digital parameters are not taken care of at all. This can be easily done by a minor extension of the data acquisition hardware. The scheme is given below.

First of all we shall require a digital multiplexer (say 8-channel digital mux 74151) to feed the digital inputs to the microprocessor one by one. The channel selection of this Mux is same as that of the analog Mux, i.e., connected to the A,B,C outputs of the timing circuit. Now since the ADC output and the digital Mux output are available to the microprocessor at the same time instant we must provide some means so that it can read them one by one. For this we delay the $\overline{CS}$ of the ADC appropriately with

the help of a D-type flip-flop. In this case connecting the clock of the D.F.F. to the 32 KHz clock of the system is sufficient which will introduce a delay of 31.25 μs. Within this time the microprocessor can read the digital Mux outputs after which it can devote itself for reading the ADC outputs. This scheme will not cause any error as the analog input of the ADC is held for a time period which is equal to the 'hold' time of the S/H amplifier, that is, 1/8 ms or 125 μ s, and the conversion time of ADC is only 15 μ s. So leaving aside 31.25 s from 125 s we have enough time for the ADC to complete the conversion and for the microprocessor to read its output value. The time period of 31.25 μs is also more than sufficient for the microprocessor to read the digital mux output. A block schematic of this scheme is given in Fig,6.1.

As regards the introduction of protocols one can consider the standard bit - oriented synchronous HDLC/SDLC protocols. Detailed description of SDLC & HDLC protocols are given in:

(i) IBM Synchronous Data Length Control General Information, GA 27-3093-1.

(ii) IBM 3650 Retail Store System Loop Interface OEM Information, GA27-3098-0.

Lastly, it should be mentioned here that SSMA (Spread Spectrum Multiple Access) techniques can also be used

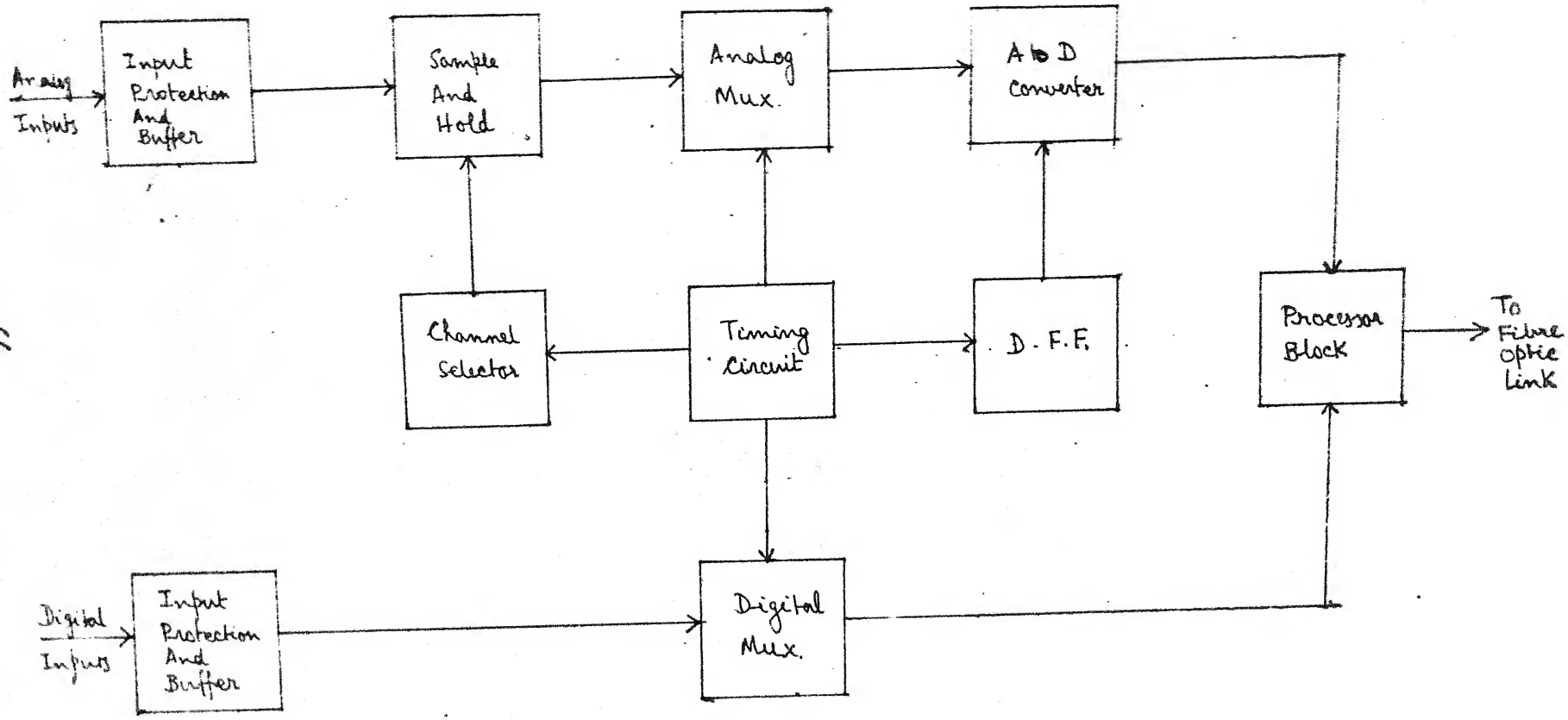

Analog Inputs
Input Protection And Buffer
Sample And Hold
Analog Mux.
A to D Converter
Channel Selector
Timing Circuit
D.F.F.
Processor Block
To Fibre optic Link
Digital Inputs
Input Protection And Buffer
Digital Mux.

Fig. 6.1

effectively for reliable transmission of data between the transmitter and the Receiver. In this scheme data from each transmitter is multiplied by a separate PN sequence of much higher frequency than the data rate and then transmitted over the channel. In the receiver the P-N sequence corresponding to each transmitter is available with the help of which the data is recovered. In this method the band-width requirement of the communication channel is very high, but, that is no problem when we are using the optical fibre as the link.

In this project we have only considered telemetry, i.e. acquisition of data from distributed remote units and sending them to a central master station. Work should also be done towards telecontrol, i.e., the master station sending control commands to the remote units for corrective measures that should be taken to erradicate the faults, to make the system complete. This would require two-way transmission through the F.O. link rather than the one-way transmission considered in the present case. Also to enhance the data handling capacity of the system more sophisticated processes like Intel 8086 should be used at both ends.

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5. 'A Multi-Computer Based Distributed Front End Communication Sub-system For a Power Control Centre' — D.E. Woods and R.D.Serafin IEEE Transactions on Power Apparatus and Systems, January 1982 .

6. IEEE Journal on Selected Areas in Communication, April 1983.

7. EC-85 User's Manual.

8. Data-Acquisition Databook, 1982 — Analog Devices.

APPENDIX A

PERFORMANCE OF A S/H AMPLIFIER

In the sample mode it is useful to consider that S/H's performance can be characterized by specifications similar to those of a closed loop OPAMP nonlinearity, gain error, bias current etc., but with some what slower response (gain bandwidth, slewing rate, settling time) because of the need to charge the storage capacitor.

However during sample to hold, hold and hold to sample states the dynamic nature of the mode switching introduces a number of specifications. These are given below:

1) Acqusition Time:

It is the time required by the output of the device to reach its final value, within a specified error band ($\pm$ 0.1%) after the sample command is given. This includes switch delay time, slewing time and settling time and is the minimum sample time required to obtain a given accuracy.

2) Aperture (Delay) Time:

The time required after the hold command until the switch is fully open. This delays the effective sample timing with rapidly changing input signals.

3) Aperture Uncertainty:

This is the range of variation in the aperture time. If the aperture time is 'tuned out' by advancing the hold command by a suitable amount, this establishes the ultimate timing error, hence the maximum sampling frequency to a given resolution.

4) Droop:

This is the change in the output voltage from the hold value as a result of device leakage or bias current flowing through the storage capacitor. Its polarity depends on the source of the leakage current within a given device. Droop rate may be calculated from droop current using the following formula:

$$\frac{V}{T} \text{ (Volts/sec.)} = \frac{I(pA)}{Ch(pF)}$$

5) Feed Through:

This is the component of the output which follows the input after the switch is open, or the a.c. input waveform that appears at the output in the hold mode. It is caused by the stray capacitive coupling from the input to the storage capacitor principally across the open switch. As a percentage of the input feed through is determined as the ratio of the feed through capacitance (Cf) to the hold capacitor (Ch).

6) Charge Transfer:

This is the charge transferred to the holding capacitor from the interelectrode capacitances of the switch when the unit is switched to the hold mode. The charge transfer generates a sample to hold offset where:

$$\text{S/H offset (V)} = \frac{\text{Charge (pC)}}{\text{Ch (pF)}}$$

7. Sample to Hold Offset:

This is the component of D.C. offset independent of Ch. This offset may be nulled using a null pot, however, the offset will then appear during the sampling mode, since it is unpredictable in magnitude and may be a function of the signal. It is also known as offset nonlinearity.

Refer to Figs. A.1, A.2, A.3 and A.4.

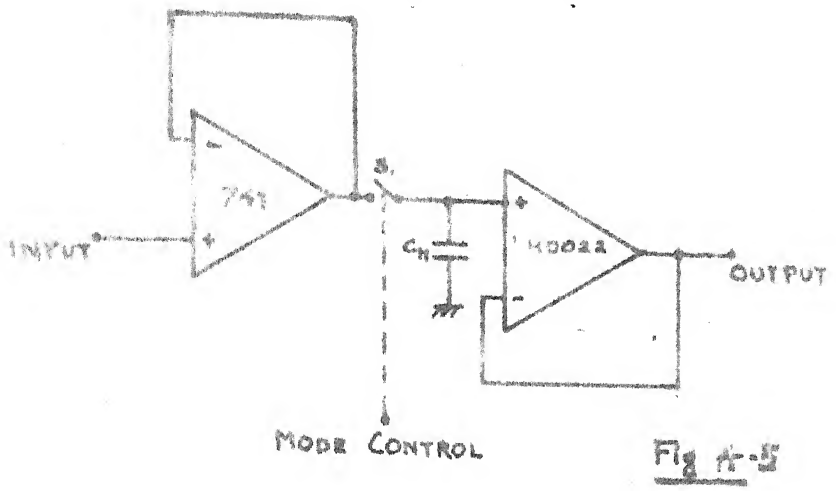


Fig A-5

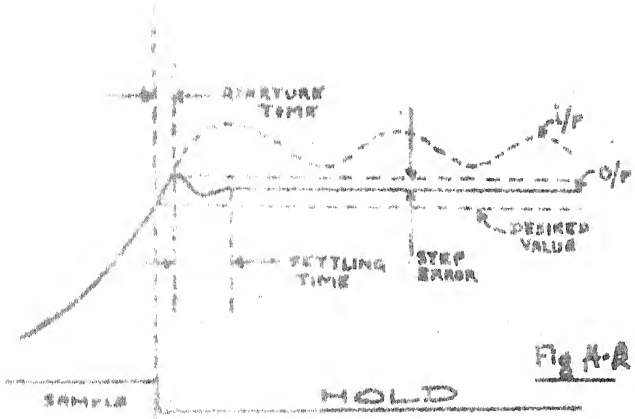


Fig A-2

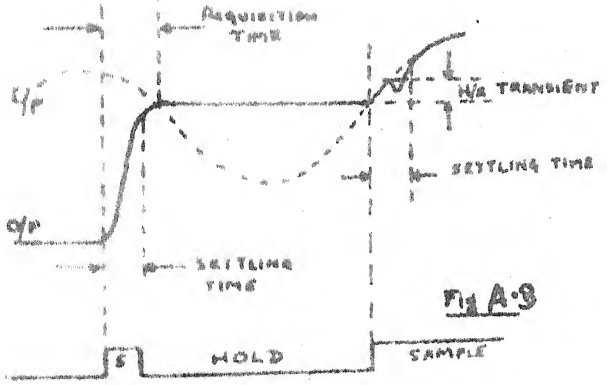


Fig A-3

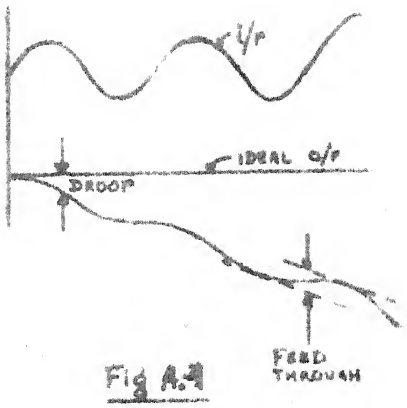


Fig A-4

APPENDIX B

BRIEF DESCRIPTION OF THE EC-85 MICROPROCESSOR-KIT

B.1 System Components

Figure B.1 shows the EC-85 printed circuit board. The components and their locations are marked in this figure. A list of the Large Scale Integrated Circuits (LSIs) along with their brief functional description is given below. A detailed description of these LSIs can be found in Intel MCS-85 User's Manual.

	Component	Functional Description
1.	8085	This is the microprocessor on which the complete system is based. It operates at the basic clock frequency of 2 MHz which is derived by internally dividing the 4 MHz crystal frequency by 2.
2.	8212.1	8212.1 is an 8 bit address latch which is used to demultiplex the lower order address information. ALE signal is used to latch the address information.
3.	8212.2	Optional Extra 8212.2 is used to buffer the 8 bit sisnals A15-A8.
4.	138.1	74 LS 138.1 is a 3 to 8 line decoder which is used in this system to provide chip select to various I/O and peripherial ICs in the system.

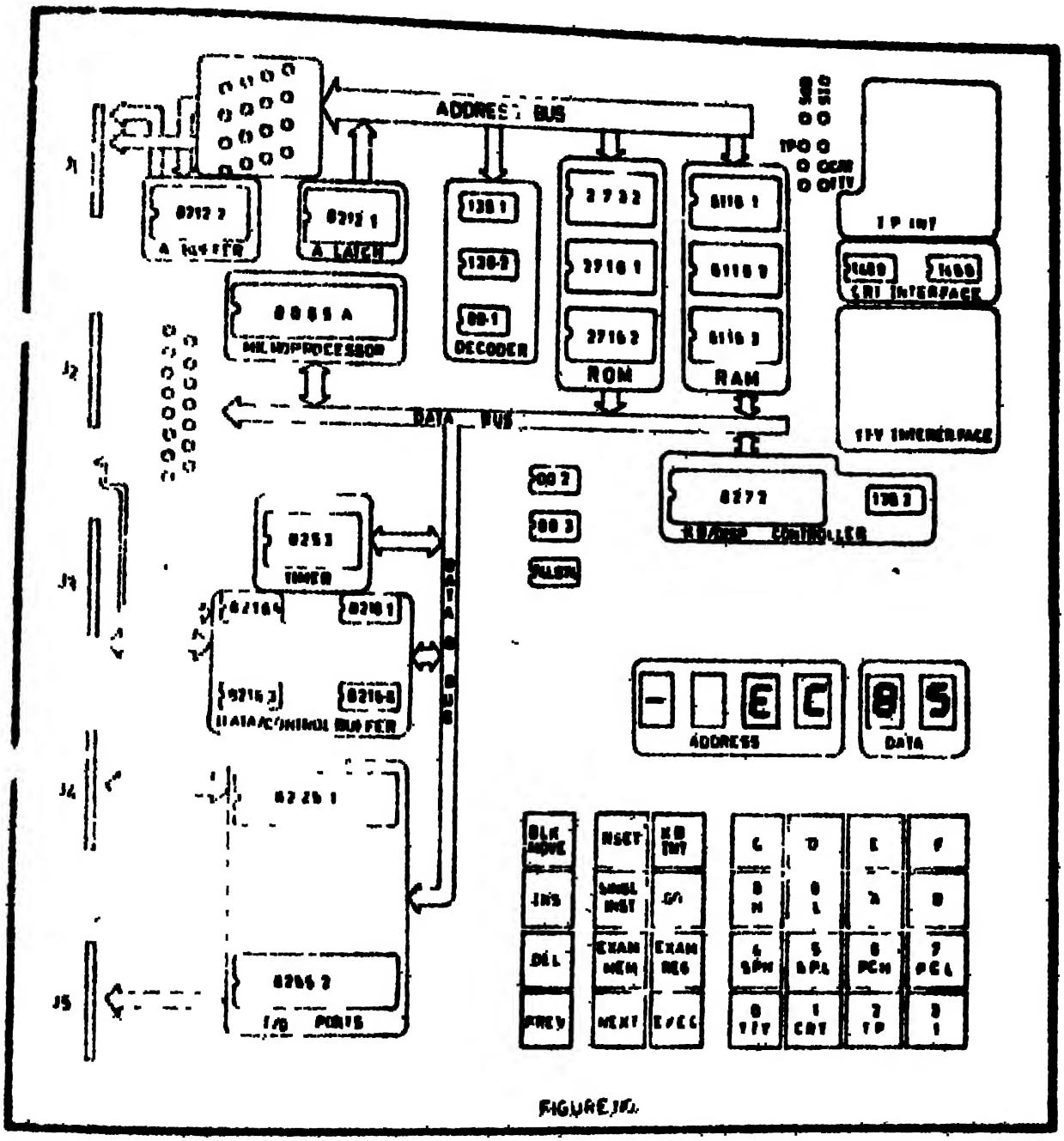

ADDRESS BUS
8212 2
A BUFFER
8212 1
A LATCH
8085 A
MICROPROCESSOR
138 1
138-2
DECODER
2732
2716 1
27162
ROM
6116 1
6116 2
6116 3
RAM
TP INT
1489
1488
RS-232 INTERFACE
TTY INTERFACE
DATA BUS
8272
138-2
FLOPPY CONTROLLER
8253
TIMER
8216
8216 1
9216 2
8216-6
DATA/CONTROL BUFFER
8255 1
8255 2
I/O PORTS
J1
J2
J3
J4
J5
ADDRESS
DATA
RESET
SINGL INST
EXAM MEM
EXAM REG
NEXT
EXEC
INS
DEL
PREV

FIGURE 10.

5.	138.2	74L S138.2 is used as a memory decoder.
6.	2732	This 4K byte EPROM stores the Monitor program.
7.	2716.1	Optional extra. This socket can be used to put a user PEROM (2716) or RAM (6116 or equivalent).
8.	2716.2	This socket can be used to put user EPROM/RAM.
9.	6116.1	2K byte Read/Write memory (RAM, 6M6). A portion of this RAM is used by the Monitor, i.e. it must not be removed or replaced by EPROM.
10.	6116.2	Optional Extra, 2K byte RAM/ROM.
11.	6116.3	Optional extra; 2K byte RAM/ROM.
12.	8253	Three 16 bit counter/timers. Counter 0 is used in the system to provide single instruction capability. Counter 1 and 2 connections are available to the user on the flat cable connectors.
13.	8216.1 to 8216.4	Optional extra. There 4 bit bidirectional buffers are used as buffers for the data bus and some of the control lines.
14.	8255.1	This chip provides 24 TTL compatible bidirectional I/O lines.

15. 8255.2 Optional extra. This chip provides additional 24 I/O lines.

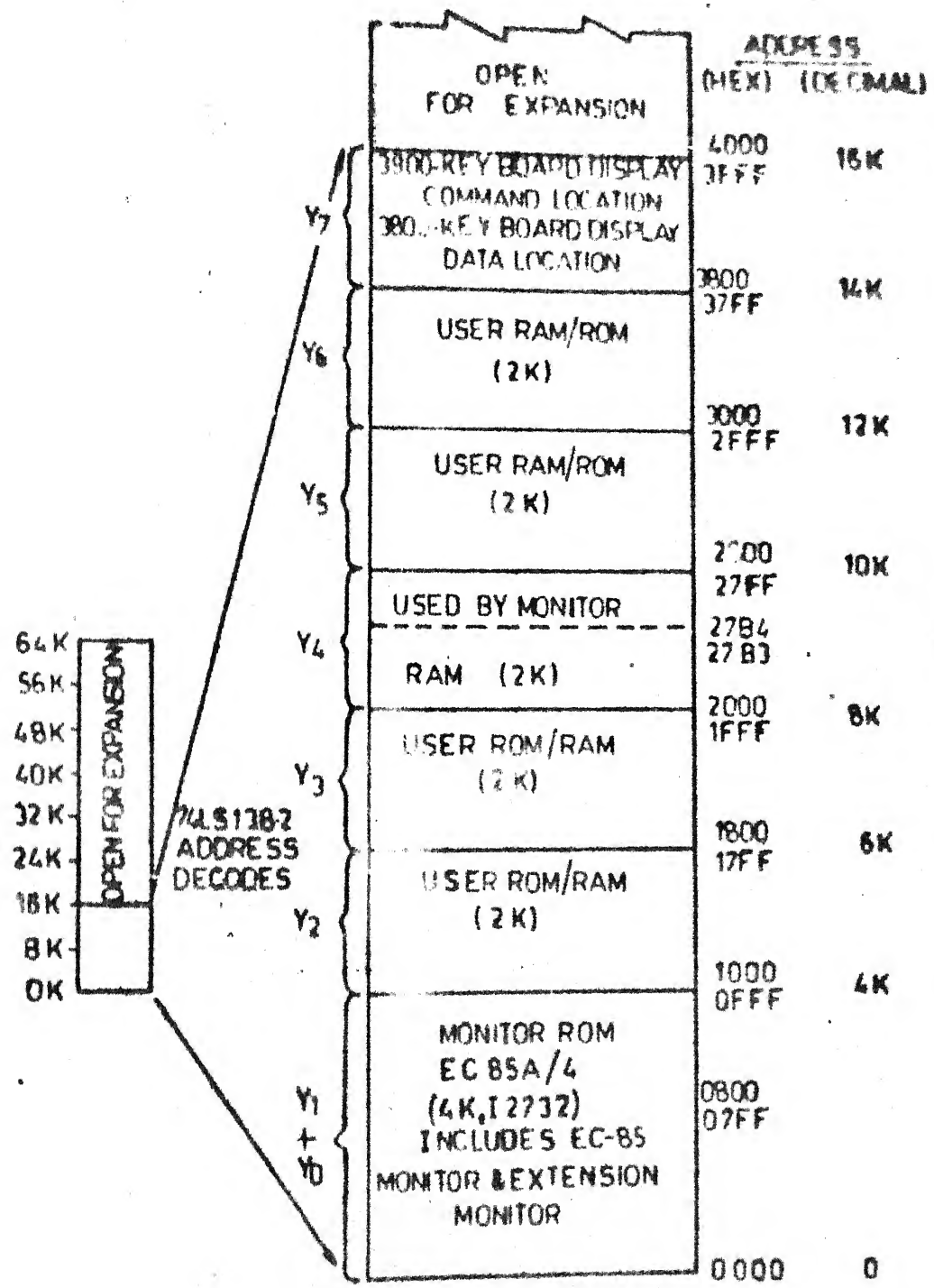
16. 8279 8279 is the complete Keyboard/Display controller which interfaces to the system bus on one side and the Keyboard and display on the other. This chip does Keyboard scanning and display refresh without CPU intervention.

B.2 Memory Addressing

Address decoder 74LS1382 is used to provide chip select inputs to various memory devices in the system. 74LS138.2 is enabled only when IO/$\overline{M}$ is low.

A memory map of the system is shown in Fig.B.2. Note that the KB/Display controller 8279 is connected in a memory-mapped I/O mode and a set of two locations are reserved in the memory space for communication with this chip.

RAM extends from address 2000 to 27FF. Locations 27B4-27FF are reserved by the monitor for special use such as jump instructions for various interrupts. Locations 27C0-27FF are used by the monitor to store variable data. Locations 2000-27B3 are available to the user for programming.



EC-85A MEMORY MAP

B.3 Keyboard/Display Controller

8279 has two portions —— keyboard portion and the display portion. In EC-85, Keyboard portion is interfaced to the Keyboard which is organised as 4x8 matrix. As a key is pressed its corresponding code is entered in the First In First Out queue in 8279. This code can now be read by the microprocessor. The display portion of 8279 has a display RAM and refresh circuitry. In EC-85 the display RAM is organised as 8 bit locations. The data can be written in the display RAM by the microprocessor and then it is refreshed automatically by 8279.

B.4 Input/Output Port and Peripherial Device Addressing

Port Addresses:

Address decoder 74LS138.1 provides chip select signals to the various I/O and peripherial devices in the system. 74LS138.1 is enabled when IO/$\overline{M}$ signal is high. Table B.1 lists each chip enable output alongwith the I/O port address over which it is active and the peripheral device which is selected. It will be seen from this table that two addresses are associated with, each port. To avoid confusion it is advisable to use one of these addresses only throughout one program, EC-85 monitor uses the former address.

TABLE B.1

74LS138.1 Output	Active range of Port Addresses	Port Numbers	Selected Device
Y_o	00 - 07		8255.1 (PPI)
		00 and 04	Port A
		01 and 05	Port B
		02 and 06	Port C
		03 and 07	Control Word
Y_1	08-0F		825.2 (PPI)
		08 and 0C	Port A
		09 and 0D	Port B
		0A and 0E	Port C
		0B and 0F	Control Word
Y_2	10-17		8253 (Programmable Interval Timer)
		10 and 14	Counter 0
		11 and 15	Counter 1
		12 and 16	Counter 2
		13 and 17	Control Word
$Y_3 - Y_7$			Not used

B.5 Signal on the Flat Cable Connectors

Signals of the flat cable connectors J_1 to J_5 are assigned the following pin connections.

Connector J_1

Assignment	PIN	PIN	Assignment	Comments
BUF A15	1	2	BUF A 12	Address Bus
BUF A14	3	4	BUF A 11	
BUF A 13	5	6	BUF A 10	
GND	7	8	BUF A 9	
GND	9	10	BUF A 8	
GND	11	12	BUF A 7	
GND	13	14	BUF A 6	
GND	15	16	BUF A 5	
GND	17	18	BUF A 4	
GND	19	20	BUF A 3	
GND	21	22	BUF A 2	
GND	23	24	BUF A 1	
GND	25	26	BUF A 0	

Connector J_2

Assignment	PIN	PIN	Assignment	Comments
CLK 2	1	2	HLDA	Connectors for controls 1,3,5 are related to timer 2 of 8253
GATE 2	3	4	HOLD	
OUT 2	5	6	READY	
GND	7	8	BUF IO/$\overline{M}$	
GND	9	10	BUF ALE	
GND	11	12	BUF SO	
GND	13	14	BUF S1	
GND	15	16	BUF CLOCK	
GND	17	18	BUF $\overline{WR}$	
GND	19	20	BUF $\overline{RD}$	
GND	21	22	BUF $\overline{INTA}$	
GND	23	24	INTR	
GND	25	26	OPEN	

Connector J_3

Assignment	PIN	PIN	Assignment	Comments
CLK 1	1	2	BUF RESET OUT	Data bus
GATE 1	3	4	RST 6.5	Pins 1,3,5
OUT 1	5	6	RST 7.5	are related to timer 1 of
OUT 1	7	8	SID	8253
RESET IN	9	10	SOD	
GND	11	12	BUF D7	
GND	13	14	BUF D6	
GND	15	16	BUF D5	
GND	17	18	BUF D4	
GND	19	20	BUF D3	
GND	21	22	BUF D2	
GND	23	24	BUF D1	
GND	25	26	BUF D0	

Connector J_4

Assignment	PIN	PIN	Assignment	Comments
PC_1 - 4	1	2	PC_1 - 5	Parallel
PC_1 - 2	3	4	PC_1 - 3	I/O Ports
PC_1 - 0	5	6	PC_1 - 1	
PB_1 - 6	7	8	PB_1 - 7	
PB_1 - 4	9	10	PB_1 - 5	
PB_1 - 2	11	12	PB_1 - 3	
PB_1 - 0	13	14	PB_1 - 1	
PA_1 - 6	15	16	PA_1 - 7	
PA_1 - 4	17	18	PA_1 - 5	
PA_1 - 2	19	20	PA_1 - 3	
PA_1 - 0	21	22	PA_1 - 1	
PC_1 - 6	23	24	PC_1 - 7	
GND	25	26	GND	

Connector J_5

Assignment	PIN	PIN	Assignment	Comments
PC_2 - 4	1	2	PC_2 - 5	Extension Parallel I/O Ports
PC_2 - 2	3	4	PC_2 - 3	
PC_2 - 0	5	6	PC_2 - 1	
PB_2 - 6	7	8	PB_2 - 7	
PB_2 - 4	9	10	PB_2 - 5	
PB_2 - 2	11	12	PB_2 - 3	
PB_2 - 0	13	14	PB_2 - 1	
PA_2 - 6	15	16	PA_2 - 7	
PA_2 - 4	17	18	PA_2 - 5	
PA_2 - 2	19	20	PA_2 - 3	
PA_2 - 0	21	22	PA_2 - 1	
PC_2 - 6	23	24	PC_2 - 7	
GND	25	26	GND	

NOTES:
1. PX_n-M stands for bit M of port X of 8255 No.n.
2. BUF stands for buffered.
3. The ground pins in the above connectors are directly connected to the ground of the corresponding ICs from which the signals are coming to the connectors.

APPENDIX C

SOFTWARE LISTING

C.1 Transmitter Software

```
        MVI A,56
        OUT 13
        MVI A,10
        OUT 11
        MVI A,00
        OUT E1
        OUT E1
        OUT E1
        MVI A,40
        OUT E1
        MVI A,FD
        OUT E1
        MVI A,13
        OUT E1
        MVI A,9B
        OUT 03
NEXT:   CALL STORE1
        STA 2700
        CALL STORE1
        STA 2701
```

```
TRY1 :    CALL    STORE1
          LXE     H,2701
          CMP     M
          JNC     STILL1
          LDA     2701
          DCX     H
          CMP     M
          JNC     FOUND1
          JZ      FOUND1
STILL1:   MOV     B,M
          MOV     M,A
          DCX     H
          MOV     M,B
          JMP     TRY1
FOUND1:   CPI     EC
          JNC     ERROR1
          JZ      ERROR1
          CP1     CC
          JNC     ERROR2
          CPI     B2
          JC      ERROR3
          JMP     NEXT1
ERROR1:   MVI     A,5A
          OUT     EO
          JMP     NEXT1
```

```
ERROR2 :    MVI    A,6A
            OUT    E0
            JMP    NEXT1
ERROR3:     MVI    A,7A
            OUT    E0
NEXT1 :     MVI    D,00
            CALL   STORE2
            STA    2704
            CALL   STORE2
            STA    2705
TRY2 :      CALL   STORE2
            LXI    H,2705
            CMP    M
            JNC    STILL2
            LDA    2705
            DCX    H
            CMP    M
            JNC    FOUND2
            JZ     FOUND2
STILL2 :    INR    D
            MOV    B,M
            MOV    M,A
            DCX    H
            MOV    M,B
            JMP    TRY2
```

```
FOUND2 :    LXI     H,2706
            MOV     M,D
            CPI     EC
            JNC     ERROR4
            JZ      ERROR4
            CPI     CC
            JNC     ERROR5
            CPI     B2
            JC      ERROR6
            JMP     NEXT2
ERROR4 :    MVI     A,8A
            OUT     E0
            JMP     NEXT2
ERROR5 :    MVI     A,9A
            OUT     E0
            JMP     NEXT2
ERROR6 :    MVI, A,AA
            OUT     E0
NEXT2 :     CALL    STORE3
            STA     2708
            CALL    STORE3
            STA     2709
TRY3 :      CALL    STORE3
            LXI     H,2709
            CMP     M
            JNC     STILL3
```

```
                LDA     2709
                DCX     H
                CMP     M
                JNC     FOUND3
                JZ      FOUND3
STILL3 :        MOV     B,M
                MOV     M,A
                DCX     H
                MOV     M,B
                JMP     TRY3
FOUND3 :        CPI     EC
                JNC     ERROR7
                JZ      ERROR7
                CPI     CC
                JNC     ERROR8
                CPI     B2
                JC      ERROR9
                JMP     NEXT3
ERROR7 :        MVI     A,BA
                OUT     EO
                JMP     NEXT3
ERROR8 :        MVI     A,CA
                OUT     EO
                JMP     NEXT3
```

```
ERROR9 :    MVI     A,DA
            OUT     EO
            MVI     D,OO
NEXT3:      MVI     D,OO
            CALL    STORE4
            STA     270C
            CALL    STORE4
            STA     270D
TRY4 :      CALL    STORE4
            LXI     H,270D
            CMP     M
            JNC     STILL4
            LDA     270D
            DCX     H
            CMP     M
            JNC     FOUND4
            JZ      FOUND4
STILL4 :    MOV     B,M
            MOV     M,A
            DCX     H
            MOV     M,B
            JMP     TRY4
FOUND4 :    LXI     H,270E
            MOV     M,D
            CPI     EC
            JNC     ERROR10
```

```
                JZ      ERROR10
                CPI     CC
                JNC     ERROR11
                CPI     B2
                JC      ERROR12
                JMP     NEXT4
ERROR10 :       MVI     A,EA
                OUT     E0
                JMP     NEXT4
ERROR11 :       MVI     A,FA
                OUT     E0
                JMP     NEXT4
ERROR 12 :      MVI     A,5B
                OUT     E0
NEXT4 :         CALL    STORE5
                STA     2710
                CALL    STORE5
                STA     2711
TRY5 :          CALL    STORE5
                LXI     H,2711
                CMP     M
                JNC     STILL5
                LDA     2711
                DCX     H
                CMP     M
                JNC     FOUND5
                JZ      FOUND5
```

```
STILL5 :    MOV     B,M
            MOV     M,A
            DCX     H
            MOV     M,B
            JMP     TRY5
FOUND5 :    CPI     EC
            JNC     ERROR13
            JZ      ERROR13
            CPI     CC
            JNC     ERROR14
            CPI     B2
            JC      ERROR15
            JMP     NEXT5
ERROR13 :   MVI     A,6B
            OUT     E0
            JMP     NEXT5
ERROR14 :   MVI     A,7B
            OUT     E0
            JMP     NEXT5
ERROR15 :   MVI     A, 8B
            OUT     E0
NEXT5 :     MVI     D,00
            CALL    STORE6
            STA     2714
            CALL    STORE6
            STA     2715
```

```
TRY6 :      CALL    STORE6
            LXI     H,2715
            CMP     M
            JNC     STILL6
            LDA     2715
            DCX     17
            CMP     M
            JNC     FOUND5
            JZ      FOUND5
STILL6 :    MOV     B,M
            MOV     M,A
            DCX     H
            MOV     M,B
            JMP     TRY6
FOUND6 :    LXI     H,2716
            MOV     M,D
            CPI     EC
            JNC     ERROR16
            JZ      ERROR16
            CPI     CC
            JNC     ERROR17
            CPI     B2
            JC      ERROR18
            JMP     NEXT6
```

```
ERROR16 :   MVI   A,9B
            OUT   E0
            JMP   NEXT6
ERROR17 :   MVI   A,AB
            OUT   E0
            JMP   NEXT6
ERROR18 :   MVI   A,BB
            OUT   E0
NEXT6 :     JMP   NEXT
STORE1 :    IN    02
            ANI    01
            JZ    STORE1
            IN    01
            ANI   07
            CPI   00
            JNZ   STORE1
            IN    00
            CPI   00
            JZ    STORE1
            RET
STORE2 :    IN    02
            ANI   01
            JZ    STORE2
            IN    01
            ANI   07
            CPI   01
```

```
                JNZ     STORE2
                IN      00
                CPI     00
                JZ      STORE2
                RET
STORE3 :        IN      02
                ANI     01
                JZ      STORE3
                IN      01
                ANI     07
                CPI     02
                JNZ     STORE3
                IN      00
                CPI     00
                JZ      STORE3
                RET
STORE4 :        IN      02
                ANI     01
                JZ      STORE4
                IN      01
                ANI     07
                CPI     03
                JNZ     STORE4
                IN      00
                CPI     00
                JZ      STORE4
                RET
```

```
STORE5 :    IN      02
            ANI     01
            JZ      STORE5
            IN      01
            ANI     07
            CPI     04
            JNZ     STORE5
            IN      00
            CPI     00
            JZ      STORE5
            RET
STORE6 :    IN      02
            ANI     01
            JZ      STORE6
            IN      01
            ANI     07
            CPI     05
            JNZ     STORE6
            IN      00
            CPI     00
            JZ      STORE6
            RET
```

C.2 Receiver Software

```
MVI   A, 56
OUT   13
MVI   A,10
OUT   11
MVI   A,00
OUT   19
OUT   19
OUT   19
MVI   A,40
OUT   19
MVI   A,FD
OUT   19
MVI   A,34
OUT   19
MVI   A,00
OUT   29
OUT   29
OUT   29
MVI   A,40
OUT   29
MVI   A,FD
OUT   29
MVI   A,34
OUT   29
MVI   A,00
```

```
OUT   39
OUT   39
OUT   39
MVI   A,40
OUT   39
MVI   A,FD
OUT   39
MVI   A,34
OUT   39
MVI   A,00
OUT   49
OUT   49
OUT   49
MVI   A,40
OUT   49
MVI   A,FD
OUT   49
MVI   A,34
OUT   49
MVI   A,00
OUT   59
OUT   59
OUT   59
MVI   A,40
OUT   59
MVI   A,FD
```

```
        OUT     59
        MVI     A,34
        OUT     59
        MVI     A,00
        OUT     69
        OUT     69
        OUT     69
        MVI     A,40
        OUT     69
        MVI     A,FD
        OUT     69
        MVI     A,34
        OUT     69
        MVI     A,00
        OUT     79
        OUT     79
        OUT     79
        MVI     A,40
        OUT     79
        MVI     A,FD
        OUT     79
        MVI     A,34
        OUT     79
TX1 :   IN      19
        ANI     02
        JZ      TXL
```

```
        OUT     59
        MVI     A,34
        OUT     59
        MVI     A,00
        OUT     69
        OUT     69
        OUT     69
        MVI     A,40
        OUT     69
        MVI     A,FD
        OUT     69
        MVI     A,34
        OUT     69
        MVI     A,00
        OUT     79
        OUT     79
        OUT     79
        MVI     A,40
        OUT     79
        MVI     A,FD
        OUT     79
        MVI     A,34
        OUT     79
TX1 :   IN      19
        ANI     02
        JZ      TXL
```

```
        IN      18
        STA     27F6
        MVI     B,00
        CALL    UPDDT
        LXI     D,00FF
        CALL    DELAY
TX2 :   IN      29
        ANI     02
        JZ      TX3
        IN      28
        STA     27F6
        MVI     B,00
        CALL    UPDDT
        LXI     D,00FF
        CALL    DELAY
TX3 :   IN      39
        ANI     02
        JZ      TX4
        IN      38
        STA     27F6
        MVI     B,00
        CALL    UPDDT
        LXI     D,00FF
        CALL    DELAY
```

```
TX4 :   IN    49
        ANI   02
        JZ    TX5
        IN    48
        STA   27F6
        MVI   B,00
        CALL  UPDDT
        LXI   D,00FF
        CALL  DELAY
TX5 :   IN    59
        ANI   02
        JZ    TX6
        IN    58
        STA   27F6
        MVI   B,00
        CALL  UPDDT
        LXI   D,00FF
        CALL  DELAY
TX6 :   IN    69
        ANI   02
        JZ    TX7
        IN    68
        STA   27F6
        MVI   B,00
        CALL  UPDDT
        LXI   D,00FF
```

```
TX7 :   IN    79
        ANI   02
        JZ    TX1
        IN    78
        STA   27F6
        MVI   B,00
        CALL  UPDDT
        LXI   D,00FF
        CALL  DELAY
```

UPDDT: This is a monitor routine of EC-85 which display the 8 bit number stored in location 27F6.

DELAY: This routine in the monitor of EC-85 takes a number in D,E and counts it down to 0.